Deep Learning-Based 3-D Inductance Extraction of Interconnects

Xiaofan Jia[(1)], Mingyu Wang[(1)], and Abdulkadir C. Yucel[(1)]

(1) Nanyang Technological University, Singapore (xiaofan002@e.ntu.edu.sg, mingyu003@e.ntu.edu.sg, and acyucel@ntu.edu.sg)

The prototyping of integrated circuits and packages can be conveniently performed via voxel-based virtual fabrication environments. Such environments allow iteratively exploring the designs and can allow checking whether the designs satisfy certain performance metrics. The designers utilizing these environments are often in need of fast and accurate parameter extraction simulators, such as inductance, capacitance, and impedance extractors. The literature abounds with physics-based parameter extractors, including the ones tailored for the voxel-based virtual fabrication environments such as (A. C. Yucel, I. P. Georgakis, A. G. Polimeridis, H. Bağcı and J. K. White, "VoxHenry: FFT-Accelerated Inductance Extraction for Voxelized Geometries," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, issue 4, 2018) and (M. Wang, C. Qian, J. K. White and A. C. Yucel, "VoxCap: FFT-Accelerated and Tucker-Enhanced Capacitance Extraction Simulator for Voxelized Structures," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, issue 12, 2020). That said, these extractors are computationally expensive, especially when their repetitive execution is required during the iterative design explorations. To tackle this issue, recently, a deep learning algorithm has been proposed to extract the capacitances of the interconnects in real-time (D. Yang, W. Yu, Y. Guo and W. Liang, "CNN-Cap: Effective Convolutional Neural Network Based Capacitance Models for Full-Chip Parasitic Extraction," *Proc. ICCAD*, 2021, pp. 1-9). In particular, a pattern matching-based simulator implementing a residual neural network was trained and used to extract the capacitance of interconnects modeled by only their 2-D cross-sections. Nevertheless, to the best of our knowledge, no deep learning-based simulator has been investigated for the inductance extraction of 3-D interconnects so far.

This study proposes a deep learning-based algorithm utilizing a 3D U-net (Ö. Çiçek, A. Abdulkadir, S. S. Lienkamp, T. Brox, and O. Ronneberger, "3D U-Net: Learning Dense Volumetric Segmentation from Sparse Annotation," *Proc. MICCAI*, pp. 424-432, 2016) to compute the inductances of 3-D interconnects. For a given structure, the proposed network takes the skin depth map and a geometry identifier distinguishing passive and active interconnects and ground planes as inputs, and provides the current density distribution on the interconnects and ground plane as the output. The currents on the ports predicted by the proposed network are then used to compute the self resistances and self and mutual inductances of interconnects. The training of the network is guided by a specially tailored loss function that allows giving more emphasis to the accurate construction of the currents on ports. The proposed network is trained and tested with a variety of structures with/without ground planes, including single interconnects, parallel interconnects, cross interconnects with random positions and different cross-sections. Preliminary results show that the proposed network can extract the parameters accurately with less than 2% error for self inductance, 5% for mutual inductance, and 6.6% for self resistance. Furthermore, it requires milliseconds to extract the inductance of interconnects, while the physics-based simulators require minutes for the same task. The architecture of the 3D U-net as well as the performance metrics demonstrating the accuracy and efficiency of the proposed network will be presented in the talk.