Design and Characterization of Radiation-Tolerant CMOS 4T Active Pixel Sensors

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***Abstract*—The design and radiation characterization of pinned photodiode 4T Active Pixel Sensors (APS) is presented in this paper. Four types of pixel layout are characterized and irradiated by 60Co γ-rays up to 170krad(Si). A variety of radiation hardening techniques are applied in these pixels. The variations between the four pixels allow us to optimize the design parameters for radiation hardness. Our experimental results exhibit increase in dark current and its non-uniformity after radiation. It is also found that Enclosed Layout Transistor (ELT) transfer gate (TX) becomes the major cause of the dark current increase. The dark current increase attributed to the shallow trench isolation (STI) around the photodiode can be mitigated by recessed-STI photodiode structure when the total dose is low. Large floating diffusion (FD) shows more immunity to the radiation-induced leakage current and random noise.**

I. Introduction

CMOS image sensors (CIS) for space and scientific applications are inherently susceptible to Total Ionizing Dose (TID) effects due to ionizing radiation. Radiation-induced degradation mechanism has been extensively studied[1][2][3]. Dark current increase has been a major observed degradation in irradiated CIS [4][5]. Ionizing radiation is known to induce charge trapping and increase interface states inside oxide isolation[6]. Charge trapping in STI may form a parasitic inversion region surrounding the photodiode, which results in the dramatic increase of the dark current. Moreover, charge trapping in gate oxide as well as channel edges of NMOS transistors can undesirably cause leakage current. Leakage current arises from the increased surface generation/recombination rate due to the formation of interface states. These are energy levels within the bandgap of the silicon, located at the silicon-oxide interface, so that they can communicate with the carriers in the silicon. Wherever interface states are in a depletion region, they result in electron-hole pair generation, leading to dark current and leakage.

In this paper, we present the design and characterization of radiation-tolerant CMOS 4T APS pixel architecture for space imaging application. We have proposed four pixel layout variation in order to find the optimized parameter settings for radiation tolerance. Within these variations, a variety of radiation-hardening techniques have been employed, such as: critical transistors in the pixel are designed using enclosed layout transistor (ELT) and P+ guard ring; the N implant for the pinned photodiode is spaced from the STI in order to prevent the photodiode junction from interaction with the defective sidewalls and edge; floating diffusion was carefully sized to deal with leakage current. A test chip including four arrays of designed pixels have been fabricated and characterized. The design perspectives of the sensor have been reported in [7]. The rest of the paper is organized as follows: the proposed pixel design in term of radiation tolerance is reported in detail in Section II. VLSI implementation and experimental results are described in Section III. Finally, concluding remarks and perspectives are given in Section IV.

II. Radiation-Tolerant Pixel Design

The schematic and cross-section details of the photosensing area is shown in Fig. 1(a), which represents a conventional 4T APS. It consists of four transistors, namely transfer gate (TX) , reset (RST), source follower (SF) and row select (RSL), respectively. In particular, it features a pinned photodiode (PPD), which acts as a potential well for collecting photo-generated charges. The drain side of TX transistor, that is the floating diffusion (FD), is the readout node where the photo-generated charges in the PPD are transferred and converted to a voltage signal. Along the charge transfer path, PPD and FD are the two critical nodes that are sensitive to radiation induced defects.

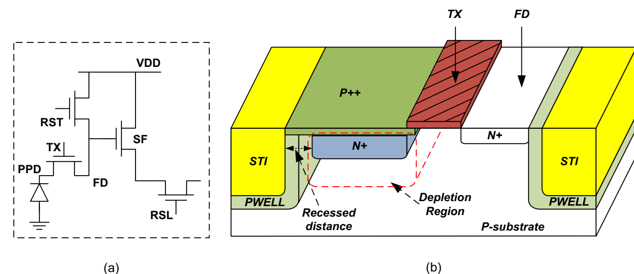

Fig. 1. (a) Pixel schematic and (b) cross-section details of the pinned photodiode.

The cross-section details of the pinned photodiode are illustrated in Fig. 1(b). The pinned photodiode can be described as N/P-sub photodiode with a thin P+ pinning layer. For the purpose of preventing from the surface defects, the doping concentration of the thin P+ layer on top of the N region is high enough to prevent the depletion region from reaching the

TABLE I
SUMMARY OF THE PIXEL CONSTITUTIONS FOR FOUR DESIGNED PIXEL TYPES

Type	RST		TX		PD			FD	SF	RSL
	Layout	W/L($\mu m/\mu m$)	Layout	W/L($\mu m/\mu m$)	C(fF)	Perim.(μm)	Area(μm^2)	C(fF)	W/L($\mu m/\mu m$)	W/L($\mu m/\mu m$)
Pixel0	ELT	3.58 / 0.43	normal	1.06 / 0.70	8.17	13.2	10.45	4.53	0.35 / 0.50	0.40/0.40
Pixel1	ELT	3.58 / 0.43	normal	1.06 / 0.70	8.17	13.2	10.45	9.94	0.35 / 0.50	0.40/0.40
Pixel2	ELT	3.58 / 0.43	ELT	3.31 / 0.77	8.81	17.7	11.34	4.23	0.35 / 0.50	0.40/0.40
Pixel3	normal	0.50 / 0.40	normal	1.06 / 0.70	10.78	16.5	14.54	2.41	0.35 / 0.50	0.40/0.40

surface oxide. Moreover, N region is deliberately spaced from the STI-sidewalls at the peripherals of the pinned photodiode. In addition, the pinned photodiode is further protected by the P-well structure. The P-well structure encloses the STI-sidewalls around the pinned photodiode. Since the doping concentration of the P-Well region is relatively higher than that of N doping region of the photodiode, STI-sidewalls is also isolated from the depletion region. The recessed-STI pinned photodiode does not touch any oxides and leads to high immunity to radiation degradation at the cost of reduced well capacity (fill factor).

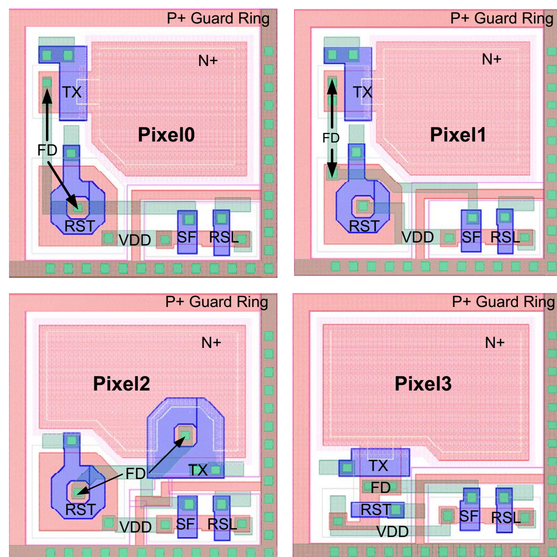

Fig. 2. Layout of the pixel configurations, namely: pixel0, RST transistor in ELT, inner-ring node used for FD; pixel1, RST transistor in ELT, outer-ring node used for FD; pixel2, both RST and TX transistor in ELT, inner-ring node used for FD; pixel3, conventional layout.

Four different pixel configurations based on the pinned-photodiode 4T APS are proposed as shown in Fig. 2. The device parameters of the four pixel configurations are summarized in Table I. All the four pixels feature the an equal pixel size of $6.5 \times 6.5\mu m^2$. Radiation tolerance of in-pixel NMOS transistors is achieved by layout enhancement, such as Enclosed Layout Transistor(ELT) and P+ guard ring. $Pixel0$ and $Pixel1$ have similar layout except the capacitance of the FD node, by swapping the source and drain of an ELT transistor. Post-layout extraction shows that the FD capacitance in $Pixel1$ is more than twice of that in $Pixel0$. $Pixel2$ uses double ELT transistors on both TX and RST and both inner diffusions are used as FD. The enclosed TX results in large aspect ratios, which amounts almost three times that of conventional TX layout. Among these configurations, $Pixel3$ is a reference design without using any enclosed gate. All transistors are sized to their minimum according to the process design rule. Since radiation-induced leakage current in transistors is usually several magnitudes less than active current, SF and RSL transistors are implemented using conventional layout. P+ guard ring is applied equally for all pixel configurations. Each of the four pixel configurations is used to build a 256×256 array. In each array, two different recessed STI distance are used. The enclosure of P-Well to STI is set to 0.1μm across the array, while the space between P-Well and N+ diffusion is chosen to 0.1μm and 0.2μm, for half of the array, respectively.

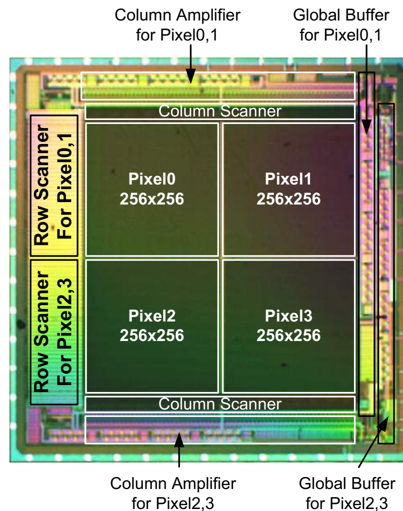

Fig. 3. Microphotograph of the prototype sensor.

III. MEASUREMENT RESULTS

A test chip including four 256×256 arrays of designed pixels has been manufactured using TSMC 0.18 μm 2P-6M CMOS image sensor process. Fig. 3 shows the microphotograph of the test chip. Each pixel sub-array has its dedicated analog readout path, which consists of two-stage analog buffers. Other peripheral circuits include timing controller and row/column scanner. The image sensor operates in rolling

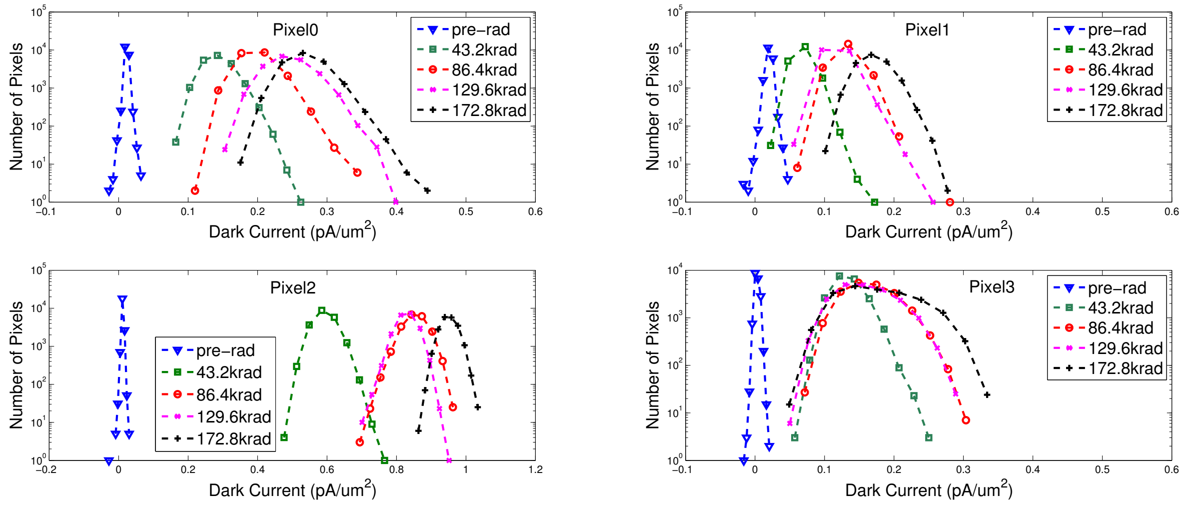

Fig. 4. Histogram of dark current as a function of radiation dose for all pixels.

TABLE II
CHARACTERIZATION SUMMARY OF EACH PIXEL TYPE

Item	Pixel0	Pixel1	Pixel2	Pixel3
Technology	TSMC 018CIS			
Pixel Type	Pinned Photodiode 4T APS			
Pixel Size	$6.5\mu m \times 6.5\mu m$			
Pixel Array Size	256 × 256			
Power Supply	3.3V			
Clock Frequency	60MHz			
Output	Analog			
Saturation Voltage(V)	1.52	1.42	1.32	1.52
RMS Random Noise($e-$)	60	44	66	84
FPN(%)	0.10	0.10	0.09	0.09
Dark Current(nA/cm^2)	2.37	1.01	5.20	1.56

shutter mode and output analog frame signals at 60MHz. The analog frame signals are converted to digital frame data by an off-chip ADC. Digital data are then temporarily stored in an Opal-Kelly XEM3010 FPGA board for image reconstruction. Since both the reset voltage and the pixel voltage are read out in each frame, digital Correlated Double Sampling (CDS) calculation is performed during the image reconstruction. The specification of the test chip is summarized in Table II.

Test chips were exposed to gamma-rays under unbiased condition at the dose rate of about 1.8krad(Si)/hour. All the pins were grounded by the conductive foam during the exposure. Four radiated samples are taken for each 24 hours. Therefore, the absorbed TID ranges from 43.2krad(Si) to 172.8krad(Si).

Fig. 4 shows the histogram of the dark current at different tested ionizing dose for all the pixel configurations. For all the pixels, the dark current is fairly low and the distribution is quite uniform before irradiation thanks to the the optimized CMOS image sensor technology. All pixel configurations exhibit dark current increase after radiation and the distribution of the pixel values spreads wider. The most significant dark current non-uniformity is observed in the reference design, $Pixel3$. The comparison between $Pixel0$ and $Pixel1$, differing only in the way FD is connected, shows that $Pixel0$ has the slower increase rate with the radiation dose. It can be inferred that the pixel with larger FD capacitance is more tolerant to leakage current caused by radiation degradation. Large FD capacitance is supposed to be favorable to radiation tolerant design. In addition, $Pixel2$ with additional ELT TX shows unexpected large dark current increase compared with other counterparts. It was expected that the ELT TX can curtail the leakage path under STI so as to minimize the radiation-induced edge leakage. However, the TX transistor used in this CMOS technology has a large intrinsic leakage current, which has contributed most to the dark current. It can be inferred that the TX transistor is the region where the most severe degradation occurs and the leakage current increases tremendously under TX transistor during the integration.

To investigate the radiation tolerance of recessed-STI photodiode structure, we have compared two different recessed distance within the pixel array. The distance of 0.2um and 0.3um are chosen. P-Well protection structures are used and the distance between the P-Well and STI is 0.1μm. The histogram of the dark current of both structures are illustrated in Fig. 5. Under all tested radiation level, it is observed that the structure with larger recessed distance(0.3um) has lower dark signal than that with closer spacing(0.2um). But the difference becomes smaller with increase of the radiation dose. When the radiation dose is high and up to 170krad, the histogram of both structures show no significant difference. At intense dose, the radiation-induced charge trapping seems to extend the depletion region to the STI interface for both structures, where the interface states and trapped charge densities are high enough to generate dark current. Therefore, a larger recess distance is expected in the presence of higher radiation dose.

Dark random noise is found to increase with radiation, as shown in Fig. 6. This is primarily because the increased

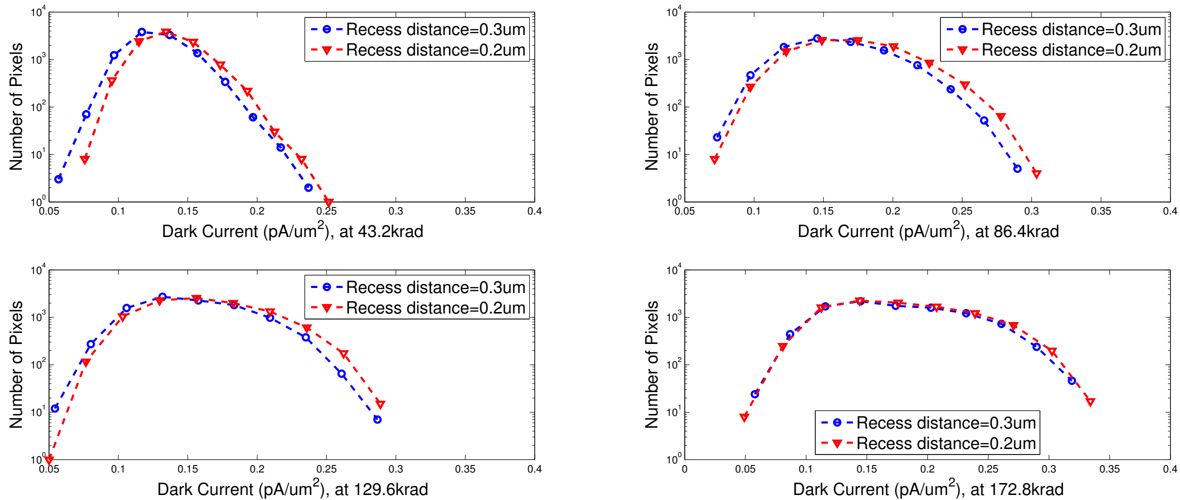

Fig. 5. Histogram of dark current regarding recessed distance in recessed-STI structure.

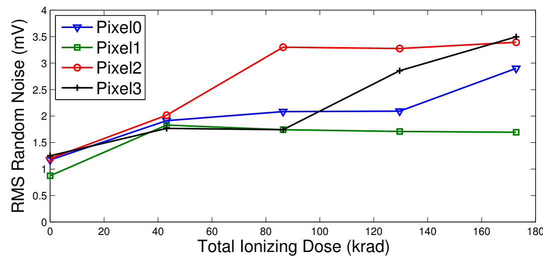

Fig. 6. RMS dark random noise increase as a function of total ionizing dose for all pixel configurations.

generation of radiation-induced interface states in the transistors. Since SF and RSL are identical for all the pixels, it is expected that the difference of the dark random noise increase arises from the TX and RST transistors with associated FD region. $Pixel2$ with the largest TX has demonstrated the most significant random noise increase. It appears that TX can generate random noise charges during integration. The degradation is probably due to the interface traps beneath the TX and the overlapping region between the PPD and TX is a major dark current source. The amount of noise charges is related to the size of TX. As is observed among all pixels, $Pixel1$ has shown the smallest dark random noise increase. This is probably because the largest capacitance at the FD has suppressed the contribution of the randomly-generated charges of these interface traps to the readout signal.

IV. Conclusion

In this paper, we have designed and characterized pinned photodiode 4T APS for space applications. In order to optimize the design parameters with regard to radiation tolerance, we have varied four different configurations from layout perspective. The radiation-tolerant 4T APS applies radiation hardening techniques primarily in PPD and FD regions. Recessed-STI structure is used for PPD. ELT layout enhancement is selectively applied to critical TX and RST. A test chip including these four sub-arrays of 256 $\times$256 pixels was fabricated using the TSMC 0.18 μm CIS process. According to the radiation characterization, TID degradation induces dark current increase. FD node is supposed to hold large capacitance so as to be less sensitive to the junction leakage current. Recessed-STI structure reduces dark current effectively at lower dose and a larger recess distance is expected when the pixel is exposed to high radiation dose. Although the ELT TX is expected to curtail the edge leakage from FD to PPD, it has demonstrated a tremendous dark current rise compared with other counterparts. Around 170krad(Si) radiation dose, TX and its associated region become the main degradation mechanism in generating dark current.

V. Acknowledgements

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