A Global-Shutter Centroiding Measurement CMOS Image Sensor with Star Region SNR Improvement for Star Trackers

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Abstract-A star tracker is a critical sensor for determining and controlling the attitude of a satellite. It utilizes a CMOS active pixel sensor (APS) to map the star field onto the focal plane. Starlight is measured and star centroids are calculated to estimate attitude knowledge. In this paper, we present a CMOS image sensor for star centroid measurement in star trackers. To improve sensitivity to low-level starlight, the capacitive transimpedance amplifier (CTIA) pixel is used as the detector. To improve centroiding accuracy, the proposed sensor architecture allows "star" pixels, pixels that are above a star threshold, to cluster together. The mean value of all the pixels in this cluster is calculated. The star signals are then amplified in relation to this mean value. This increases the signal-to-noise ratio (SNR) in star regions in line with their starlight intensity. An adaptive region-of-interest (ROI) readout architecture is also proposed, which reports only stars regions, instead of the entire frame. The proof-of-concept chip, containing a 128×128 pixel array, was fabricated using AMS 0.35 μ m CMOS Opto process. Each pixel has a size of 31.2×31.2 μ m². The measurement results show that centroiding accuracy increases with higher centroiding gain. Within a limited exposure time, the relative centroiding accuracy can surpass that of a commercial image sensor by more than 1%.

Index Terms—Complementary metal-oxide semiconductor (CMOS) image sensor, star sensor, star tracker, capacitive transimpedance amplifier (CTIA), low-light imaging.

I. INTRODUCTION

Attitude knowledge is important for modern space platforms. It must be measured and controlled for a variety of operations, such as, pointing solar panels at the sun, pointing a high-gain communications link towards a ground station or attitude acquisition for a scientific payload. These missions requiring high attitude precision naturally imply a need for high-accuracy sensors. Modern space platforms are usually equipped with a star tracker capable of offering bore sight accuracy in terms of arcseconds [1]. Star trackers are more accurate than any other state-of-the-art attitude sensing technologies such as magnetometers, gyroscopes, sun sensors and earth horizon sensors.

Fig. 1 shows the block diagram for a typical star tracker. The device mainly consists of a set of telescope optics and an



Fig. 1. Block diagram of a typical star tracker.

image sensor in conjunction with signal processing electronics. The CMOS image sensor captures a star map (image). The centroids of the detected stars are extracted and computed to build up a star pattern and the recognition algorithm searches the pattern in the star-catalog to finally determine the attitude [2]. Regardless of the algorithmic accuracy in the signal processing and recognition phase, the star tracker's performance will heavily depend on its centroiding accuracy and, in turn, on its starlight measurement precision [3–6]. The effects on centroiding accuracy of various noise components in CMOS active pixel sensors (APS) are discussed in [7]. From the system-level design perspective, it is necessary to increase the signal-to-noise (SNR) ratio of the star pixels in order to achieve high centroiding accuracy.

Detecting a limited number of photons generated by stars is a challenging task for conventional 3-Transistor APS, especially when integration time is also limited [8]. Due to the direct charge accumulation on the photodiode, the large photodiode capacitance results in a small voltage change, and thus low sensitivity. Also, it is difficult to perform correlated double sampling (CDS) to suppress the reset noise in a 3-Transistor APS [9], rendering the SNR unsuitable when high centroiding accuracy is required. To overcome these drawbacks and to achieve better sensitivity many different pixel structures have been proposed in the past. In a 4-Transistor APS, the charge-to-voltage conversion is made on a separate floating diffusion node which gives rise to higher sensitivity and enables CDS operation to cancel the reset noise. Single photon avalanche diode (SPAD) is another pixel structure to provide high sensitivity [10, 11]. It outputs a digital pulse in response to absorbing a single photon, which is usually the result of a reflected beam of laser from an active measurement system such as the Time-of-Flight (ToF) range finder [12, 13]. Yet another high sensitivity pixel is the capacitive transimpedence amplifier (CTIA) pixel [14–18]. In CTIA pixel, the photodiode charges are accumulated on a separate capacitor. This capacitor can be smaller than the photodiode capacitance which results in high conversion gain and improved sensitivity.

Low-noise column-level signal processing circuits also play an important role in suppressing the various noises[19] for better SNR. High-gain column-level amplifiers are widely used to cancel out reset noise [20, 21]. They can also reduce thermal pixel source follower noise by a factor of the square root of the gain and wideband output buffer noise by a factor of the gain [22].

This paper presents a CMOS image sensor for star tracker application. It uses the CTIA pixel and column-level signal processing to achieve high SNR. The main contribution of this work is a sensor architecture specially optimized for star tracker with improved star centroid measurement accuracy. We propose a focal-plane algorithm for SNR improvement in star regions. The sensor is able to segment star regions from the background by means of adaptive star thresholding. In each star region, the mean value of all the star pixels is calculated. The difference between the star signals and this mean value is then amplified, effectively increasing the SNR. The rest of the paper is organized as follows: Section II introduces a detailed system analysis for the sensor design; Section III describes the sensor architecture and circuit designs; Section IV presents the sensor implementation and measurement results and some conclusions are drawn in Section V.

II. SYSTEM ANALYSIS

Fig.2 shows how a star sensor maps the star field onto the focal plane. Due to the lens point spread function (PSF), star energy will typically spread over several neighbouring pixels and form a star spot. The pixel responses in a 5×5 region-of-interest (ROI) are highlighted. The star centroid can be calculated using the center-of-mass [1] as follows:

$$\begin{cases} x_c = \sum_{i,j} x_{ij} S_{ij} / \sum_{i,j} S_{ij} \\ y_c = \sum_{i,j} y_{ij} S_{ij} / \sum_{i,j} S_{ij} \end{cases}$$
(1)

where (x_c, y_c) represents the calculated centroid coordinate and S_{ij} is the signal magnitude at pixel(i,j) in the ROI. Using this hyperacuity technique, a star's position can be identified down to a sub-pixel level of accuracy [23]. The deviation of S_{ij} from its ideal value due to various sensor noises will lead to a deviation in the calculated centroid. The centroiding error is inversely proportional to the SNR of S_{ij} [24]. Increasing the SNR can effectively improve the centroiding accuracy. The signal quality can be improved by increasing integration time, using high sensitivity pixel or applying signal amplification as well as noise control techniques in the readout path.

In astronomy, star brightness is characterized as apparent magnitude (M_V). Using the Sun (M_V =-26.76 and solar flux of 1.36 KW/m²) as a reference, it is possible to derive the



Fig. 2. Focal plane for star centroid calculation.

irradiance of any other star [1]. A $M_V=0$ star has a radiation of 1.44×10^{-8} W/m². By taking into account factors such as spectral distribution, the photo-detector's quantum efficiency (QE) and the lens point spread function (PSF), it is possible to estimate the starlight power impinging on the pixel. A star tracker with a 2 cm lens aperture, 85% lens transmission efficiency, and a 1.2 pixel PSF can only produce about 80 fA at the center pixel of the star if the average photodiode responsivity is 0.3 A/W. An exposure time of 10 ms generates about 5 K photoelectrons. In a typical 0.35 μ m CMOS process, a 15 \times 15 μ m² Nwell/Psub photodiode has a capacitance of approximately 50fF. The resulting voltage change is then 16 mV. Such a limited change represents a challenge for a CMOS image sensor, particularly in a space radiation environment.



Fig. 3. Stars travel on the focal plane during integration due to the satellite's orbit. The travel distance L is expressed in pixels in one dimension, where d_{pixel} is the pixel pitch.

Increasing the integration time does not increase the signal magnitude because of the dynamic condition of the orbiting satellite [25], as shown in Fig. 3. The satellite's orbital movement causes the star spot to move in the opposite direction on the focal plane, and the resulting "tail effect" induces systematic error. The distance travelled on the focal plane can be expressed in terms of pixels as:

$$L = \frac{N_{pix} \cdot \omega \cdot T_{int}}{2\tan(FOV/2)} \tag{2}$$

where N_{pix} is the pixel number in one dimension of the pixel array, ω is the angular rate, T_{int} is the integration time



Fig. 4. (a) and (b) are simulated static star images and integration results, respectively. (c) and (d) are simulated dynamic star images and integration results with star shift, respectively. They are captured with the same integration time. When the star center moves to its neighboring pixel during integration, the star energy is spread over more pixels. The resulting "tail effect" does not increase the signal magnitude.

and FOV is the star tracker field of view. A low-earth orbit (LEO) satellite at an altitude of 600 km has an angular rate of 0.06 deg/s. For a CMOS image sensor with 1 K pixels in one dimension and 20° FOV, a 200 ms integration time can produce a shift of 0.6 pixels. With the increase of the exposure time, the starlight will gradually move away from the pixel and shift to its neighbouring pixels. Further increasing the exposure time will not increase the signal magnitude on one pixel (see Fig. 4). Instead, the incident photons will spread over more pixels and the signal magnitude will be limited by this shift. Thus constrained by integration time, the only effective way to detect weak starlight is to increase the sensitivity of the pixel.

The proposed sensor architecture uses the CTIA pixel for high sensitivity and thus high SNR. Besides, we also propose an on-chip SNR improvement algorithm to further boost the centroding performance. It can be noted from Eq. 1 that S_{ij} is the weighing factor in the centroid calculation. The differences between S_{ij} in the ROI are what matters for the centroiding performance. In other words, increasing the SNR is equivalent to increasing the signal differences in the ROI. The proposed algorithm amplifies the difference using on-chip signal processing. The algorithmic process is illustrated in Fig. 5. It can be divided into three major steps. First, the sensor locates "star" pixels on the focal plane by means of thresholding (Fig. 5(i)). A global threshold defines the boundary between the "star" and the background pixels. This threshold filters out the background and helps in segmenting the image into different "stars" regions. The block of pixels belonging to the same star region form a so-called "cluster" [26]. Second, each pixel cluster calculates the mean value of all the pixels in it (AVG1,AVG2)(Fig. 5(ii)). Each "star" will have its own mean value with respect to its starlight intensity. Third, "star" signals are amplified with their own mean value (Fig. 5(iii)). Unlike a global reference, the mean value acts like an "AC ground"



Fig. 5. Star thresholding and local average calculation. The global star threshold is used to locate star region, and the mean value is calculated within the region. In this way, each different star will have an individual mean value. This mean value is then used as a local reference for signal amplification.

and only the difference between star signals are amplified.

III. SENSOR ARCHITECTURE

The block diagram of the sensor architecture is shown in Fig. 6(a). It is composed of a 128×96 pixel array, column-level CDS and centroiding gain circuits, selective row and column scanners with address encoders and a main controller. The pixel array performs global thresholding during integration. The threshold value is controlled externally so that it can be adapted to different background levels. In the pixel array, each pixel has cluster interconnections with its four neighbouring pixels. It is also connected to two RCFG/CCFG buses. The buses are reset to high. Once a "star" is detected, the horizontal RCFG bus is pulled down and the shift register chain in the row scanner is configured. The shift register is similar to the one in [8] and can be bypassed if the RCFG bus is high. Likewise, the CCFG bus is pulled down when this row is selected during readout. The selective readout can only report the pixels in the ROI. In contrast to the WTA (Winner-Take-All) and row/column profiling architecture which detects a single ROI for a sun sensor [27], the proposed global thresholding and selective readout strategy allows the detection of multiple ROIs in the same scene. Dual to the selective readout, the configuration latch in the shift register can also be overridden by the external command to force a sequential scan so that the sensor can also output a snapshot frame. Correlated Double Sampling (CDS) and star signal amplification are performed in column-level circuits.



Fig. 6. (a) Block diagram of the sensor architecture. Schematic of (b) pixel circuits and (c) reset switch.

A. Pixel Circuits and Operation

Fig. 6(b) shows the schematic of pixel circuits. In CTIA pixel, the photodiode voltage is held at a constant value by the OTA so the photoelectrons will flow to discharge the integration capacitor. If the OTA has sufficiently high open-loop gain, the output of the OTA will follow:

$$V_o \approx \frac{1}{C_{\rm int}} \int I_{ph} dt \tag{3}$$

where I_{ph} is the photocurrent. The reset switch is a T-type switch, as shown in Fig. 6(c). It consists of three NMOS transistors and an inverter. The node V_m is tied to an externallyproduced bias voltage (V_{im}) close to V_i during integration. So the leakage path from V_o to V_i is eliminated when V_o builds up. Otherwise, a single NMOS transistor would inject a subthreshold leakage current from output of the OTA to the photodiode. This leakage current can be as large as the photocurrent in low-light condition. The same switch structure is also applied to SH0 to eliminate the subthreshold leakage, because V_{rst} must be held on C0 for the entire integration time before it is read out. The OTA is a two-stage seventransistor operational amplifier. Three NMOS capacitors (C0, C1, C2) are used as analog memories to temporarily store the pixel values V_{rst} , V_{sig} and V_{avg} , respectively. Each capacitor is connected to a source follower to drive a column bus. The latched-type comparator compares V_{siq} with global threshold V_{star} . The comparison result, denoted as flag, controls four switches that connect to its four neighbour pixels. It also controls the switches that pull down the RCFG bus and CCFG bus.

The timing diagram of the pixel operation is shown in Fig. 7. Initially, the pixel array is globally reset. To cancel the reset noise, SH0 is turned off slightly after pixel reset and the reset level of the CTIA pixel, including the negative charge injection of the reset switch, the reset noise and the OTA offset, is sampled on C0 (at T0). During integration, once V_{sig} is larger

than V_{star} , the comparator toggles and raises flag turning on the pass switches to its four neighbouring pixels. If its neighbouring pixels also triggers flag, a connection is formed (e.g. pixel A and pixel B at T1). Pixel-to-pixel connections can be formed till the end of the integration time, T2 after which we will have "star" pixel clusters throughout the pixel array. When MG is turned on at T3, charges on C2 of all connected pixels are merged and the mean level of each pixel cluster is calculated.

B. Pixel Implementation

Fig. 8 shows the layout of the pixel. The top routing layers (M3 and M4) are not shown for clarity. The pixel has the footprint of 31.2 μ m \times 31.2 μ m. The placement and routing are carefully designed to minimize the silicon area for pixel circuits. This is for the purpose of increasing the photodiode size as large as possible. The targeted fill factor (FF) is 30%, which is a good balance between SNR and DR on one side and spatial resolution and Modulation Transfer Function (MTF) on the other [28]. A 20 μ m×16.9 μ m N-well/P-sub photodiode is used and surrounded by the guard ring. The resulting fill factor is about 34.7%. An anti-reflective coating layer is placed above the photodiode in order to improve the responsivity. The integration capacitor is a PIP capacitor and designed to be 4.76 fF. The sampling NMOS capacitors are designed to be 25 fF. They are placed next to each other for better matching. They are also shielded from signal wires with GND metal plates. All bias and reference voltages are shared in the row and supplied from the left side of the row.

C. Pixel Noise Analysis

This section discusses the pixel noise. Major noise sources in the CTIA pixel include OTA noise, reset noise and readout noise. Inside the pixel, the noise at the output of the CTIA



Fig. 7. (a) Timing diagram and (b) operation flow of the pixel circuits. An example block diagram of 2×2 pixel array demonstrates the interpixel operation. Before integration, pixel reset values are sampled on the C0. During integration, pixels that reach star threshold make connection with its neighboring pixels. Pixels can make such connections until the end of integration. At the end of the integration, the connected pixels form a star cluster (pixel A, B and C). When the MG is turned on, charges on C2 of these pixels are merged and averaged. The local reference V_{avg} is accordingly calculated.

can be estimated as:

$$\overline{v_{no,ota}^2} = \left(1 + \frac{C_{pd}}{C_{int}}\right)^2 \overline{v_{ni,ota}^2} \tag{4}$$

where $\overline{v_{ni,ota}^2}$ is the input-referred noise power of the OTA. The reset noise on C_{int} is expressed as:

$$\overline{v_{n,rst}^2} = \frac{kT}{C_{int}} \tag{5}$$

Due to small C_{int} , the reset noise $\overline{v_{n,rst}^2}$ becomes dominant. In order to cancel it, the pixel requires to sample both the reset value and signal value onto C_{rst} and C_{sig} , respectively. This will induce additional sampling noise. The following sampling



Fig. 8. Pixel layout.



Fig. 9. Column signal path which is composed of two-stage switched-capacitor circuits.

noises are added:

$$\overline{v_{n,sh}^2} = \frac{kT}{C_{rst}} + \frac{kT}{C_{siq}} \tag{6}$$

If we make the size of both capacitors equal, that is $C_{rst} = C_{sig} = C_{sh}$. The resulting differential sampling noises are then:

$$\overline{v_{n,sh}^2} = 2\frac{kT}{C_{sh}} \tag{7}$$

The added sampling noise can be suppressed by using large C_{sh} . For example, if the sampling capacitor is designed to be 30 fF, the differential sampling noise is then 0.53 m V_{rms} at room temperature (T=300 K), about half of that of reset noise with $C_{int} = 4fF$.

Accordingly, with the cancellation of the reset noise by CDS, the input-referred noise of the CTIA pixel is then:

$$\overline{v_{n,pix}^2} = 2\left(1 + \frac{C_{pd}}{C_{\text{int}}}\right)^2 \overline{v_{n,ota}^2} + 2\frac{kT}{C_{sh}} + 2\overline{v_{sf}^2} + \overline{v_{n,col}^2}$$
(8)

where $\overline{v_{n,col}^2}$ is the input-referred noise power of the columnlevel circuits and $\overline{v_{sf}^2}$ is the noise power of the in-pixel source follower, which is dominated by the 1/f noise.

D. Column Signal Path

The circuits of the column signal path are shown in Fig. 9. The column circuit mainly has two stages of charge amplifiers and a mode multiplexer. The first stage samples V_{rst} and V_{sig} and perform CDS with gain of one. The second charge amplifier samples CDS result V_{cds} and V_{avg} and outputs the amplified star signal with variable gain. This stage has a gain of 1, 2, 4 or 8, which is controlled externally by gain select signals (G0, G1 and G2). The mode switches SM select the output of either stage. Hence, it enables either imaging mode or centroiding readout mode.

IV. MEASUREMENT RESULTS

A proof-of-concept chip was fabricated using AMS 0.35 μ m 2-poly 4-metal CMOS Opto process. Fig. 10 (a) shows the chip microphotograph where the main building blocks are highlighted. The core of the chip is 4.7 mm × 4.6 mm large. The sensor is interfaced with a FPGA test platform. The FPGA provides clock and control signals to the sensor. The system clock frequency to drive the sensor is 10 MHz. The sensor's outputs are converted to digital data by an off-chip 12-bit ADC and collected by a RAM on the test platform.



Fig. 10. (a) Chip microphotograph. (b) Centroiding measurement setup.

The sensitivity is characterized with the help of an integrating sphere. The sensor was exposed to varying illumination levels by keeping the integration time fixed (6 μ s). For each illumination level, we sampled 100 frames to obtain the averaged pixel response. The plot of average pixel response (in ADC units) versus different luminous exposures is shown in Fig. 11. The slope of the curve gives the sensitivity. The measured sensitivity is 10.9 V/lux·s. The conversion gain is 33.6 μ V/e-. The temporal noise is measured to be 3.4 mV_{rms} and the dynamic range is 55.7 dB. Other characterization results are summarized in Table I.



Fig. 11. Pixel response curve.

TABLE I Performance Summary of the Sensor

Technology	AMS 0.35 µm CMOS Opto process
Pixel Size	31.2×31.2 µm ²
Photodetector Type	N well/P sub
Photo data ato a Cina	$20 \times 10^{\circ} \text{ m}^2$
Photodetector Size	$20 \times 16.9 \ \mu m^2$
Fill Factor	34.7%
Photodiode Capacitance	64.68 fF
Photodiode Responsivity	0.32 A/W @ 632 nm
Dark Current	$1.15 \text{ fA}/\mu\text{m}^2$
Integration Capacitance	4.76 fF
Conversion Gain	33.6 µV/e-
Signal Swing	1.2 V
FPN	0.72%
Temporal Noise	$3.4 \text{ m}V_{rms}$
Sensitivity	10.9 V/lux·s
Dynamic Range	55.7 dB

The snapshot frame can be obtained by switching to imaging mode in column signal path and forcing a sequential scan in row and column scanners. Fig. 12 shows two sample images. They were captured with 4 ms integration time in ambient lighting condition (about 300 lux).



Fig. 12. Sample images in snapshot mode.



Fig. 13. Test pattern: three circular spots at equal distance on a LCD screen. (a) Pattern A: uniform profile and uniform size. (b) Pattern B: uniform profile and different size. (c) Pattern C: gaussian profile and uniform size. (d) Pattern D: gaussian profile and different size.

The centroiding test was performed in a dark room. The test setup is shown in Fig. 10(b). The test equipments are placed on an optical table. The sensor was placed behind a collimator lens. The main purpose of the collimator lens is to convert the divergent light beams from the light source (LCD screen) to become parallel to simulate starlight. Three equidistant circular spots projected from an LCD screen were used to represent a star pattern (Fig. 13). Four different patterns with different spot profiles and spot sizes were used for test purposes. For each pattern type we used both a uniform intensity profile and a quasi-gaussian intensity profile. The distance of AB or BC are 12 pixels. Each circular spot has a diameter of eight LCD pixels. Keeping the distance constant, the diameter of the rightmost spot is increased to 12 pixels for both intensity profiles (pattern B and D). These patterns were created in gray-scale images. The resolution of the image is the same as the LCD screen so as to ensure pixel-to-pixel display without any distortion or compression. The block of LCD pixels are together treated as point light sources with ground-truth positions on the LCD screen. The sensor was mounted with a lens (12 mm focal length and aperture = f/4). The lens was then slightly defocused to spread each spot over 7×7 ROI. The centroiding algorithm in Eq. 1 was applied to calculate the respective centroids. After that, we measured the relative distance error AB/BC-1 to evaluate the centroiding accuracy.

We captured 100 frames and for each frame we calculated the relative distance error. The results were averaged in order to reduce the effect of thermal noise. Fig. 14 shows the averaged relative distance error. The centroiding accuracy increases with the centroiding gain, thereby, implying that higher centroiding gain leads to higher SNR in the star region, which in turn demonstrates higher centroiding accuracy. We tested different scenarios with various background levels for the proposed sensor. Even with high background level (2/3 signal swing), it still can achieve good centroiding accuracy at higher centroiding gain.



Fig. 14. Measured relative distance error.

In addition, using the same lens and collimator, the centroiding performance was compared with a commercial CMOS image sensor "Aptina MT9M032", which is used in various star trackers [29, 30]. The optics are tuned and refocused so that the star spots are also spread in 7×7 ROIs. We have calculated relative error at three different integration times. Likewise, the results were averaged from 100 frames to reduce the effect of the thermal noise. The comparison results of different patterns are summarized in Table II. In all tested scenarios, MT9M032 shows relatively poor centroiding accuracy with short integration. The relative errors are above 1% when the integration is below 5 ms. When the integration is higher, it becomes comparable with the proposed sensor. It is primarily because MT9M032 utilizes 3T APS pixel structures which has a rather low sensitivity (2.1 V/lux-sec in monochrome mode). 5 ms is not enough for the pixel to collect enough charges to attain acceptable SNR. The proposed sensor has about 5 times better sensitivity and thus leads to better centroiding accuracy. The improvement is even larger when higher centroiding gain is applied.

 TABLE II

 Relative error [AB/BC-1] in comparison with Aptina MT9M032

	Pattern A			Pattern B		
Exp.	MT9M032	This sensor		MT9M032	This sensor	
		G=1	G=4		G=1	G=4
3 ms	1.72%	0.63%	0.31%	0.74%	0.73%	0.71%
5 ms	0.63%	0.52%	0.19%	0.58%	0.48%	0.36%
10 ms	0.12%	0.14%	0.06%	0.12%	0.12%	0.11%
	Pa	attern C		Pa	attern D	
Exp.	Pa MT9M032	attern C This s	sensor	Pa MT9M032	attern D This s	sensor
Exp.	Pa MT9M032	attern C This s G=1	sensor G=4	Pa MT9M032	attern D This s G=1	sensor G=4
Exp.	Pa MT9M032 1.53%	attern C This s G=1 0.39%	sensor G=4 0.24%	Pa MT9M032 1.62%	attern D This s G=1 0.42%	sensor G=4 0.26%
Exp. 3 ms 5 ms	Pa MT9M032 1.53% 1.04%	attern C This s G=1 0.39% 0.18%	sensor G=4 0.24% 0.13%	Pa MT9M032 1.62% 1.72%	ttern D This s G=1 0.42% 0.34%	sensor G=4 0.26% 0.15%

Table III shows the centroiding accuracy improvement with FPN cancellation. The FPN cancellation is performed by subtracting a dark reference frame. The dark frame which stores the digitized offset voltage is captured during calibration phase. It is averaged from multiple frames to eliminate the temporal noise. FPN also affects the centroiding error. Under all tested patterns, the centroiding errors decrease with FPN cancellation.

 TABLE III

 Centroiding Accuracy Improvement with FPN cancellation

Int. time	Pattern A	Pattern B	Pattern C	Pattern D
3 ms	-0.04%	-0.09%	-0.12%	-0.03%
5 ms	-0.04%	-0.09%	-0.02%	-0.02%
10 ms	-0.03%	-0.03%	-0.03%	0.00%

V. CONCLUSION

This paper presents a CMOS image sensor for centroid measurement in star trackers. To improve centroiding accuracy, a sensor architecture specially optimized for star tracker has been proposed. It enables "star" pixels, pixels that are above a star threshold, to cluster in order to calculate the mean level of all the star signals in the star. The star signals are then amplified in relation to this mean level. This increases the SNR in star regions in line with starlight intensity and irrespective of the background level. A proof-of-concept chip with a 128×96 pixel array was fabricated in a 0.35 μ m mixed-signal CMOS process. Measurement results show that the device's centroiding accuracy increases with higher centroiding gain. Compared with a commercial image sensor, its relative centroiding performance is more than 1% higher.

VI. ACKNOWLEDGEMENT

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