Nanyang Technological University

Low-Power Column-Parallel ADC for CMOS Image Sensor by Leveraging Spatial Likelihood in Natural Scene

By

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Abstract

Column-Parallel analog-to-digital converter (ADC) technology has often been integrated in CMOS Image Sensors as a system-on-chip (SoC) solution, in particular for portable devices. Since the power consumption of column-parallel ADCs in CMOS image sensors play an important role in total power consumption, a low-power application on has been developed specifically for integration in low-power image systems.

In a conventional column-parallel ADC design, the ADC operation is repeated row to row, column to column and frame to frame, regardless of the properties of the scenes. In this thesis, a new operating method is proposed, which takes into account spatial likelihood in natural scenes. In the proposed method, the MSBs of selected pixel would be predicted before the ADC operation, based on that pixel's neighbor pixels in the previous row. Because there is strong correlation between consecutive rows in most natural scenes, pre-ADC pixel estimation could save bits in ADC conversion cycles. The total number of ADC conversions would effectively be reduced, resulting in lower power consumption. This method was verified in extensive Matlab simulations, where ADC conversion cycles were reduced by up to 20%-30% for most natural scenes and a saving of up to 29.49% was achieved in switching energy for a 512×512 resolution Lena image.

This thesis presents the design of a column-parallel low-power ADC system for a CMOS image sensor with the proposed algorithm. The system was implemented in AMS 0.35 μm CMOS technology. The study also details the simulation of the algorithm and the testing of the hardware. Improvements made to the algorithm after the analysis and testing of the CMOS imaging sensor are described at the end of the thesis.

Acknowledgments

I would like to express my sincerest gratitude to my Master program supervisor, Professor Chen Shoushun, for his insight of IC design, his research methodology and inspiring thinking, his steady encouragement and guidance throughout my two-year master study. The supervision and the systematic training provided by him really helped me on exploring out the system-level design of an image sensor and critical thinking on both top level and circuit level. Besides, I am really appreciate his trust on my research working and my working ability.

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List of Abbreviations

ADC	Analog-to-Digital Converter
APS	Active Pixel Sensor
CMOS	Complementary Metal-Oxide-Semiconductor
CIS	CMOS Image Sensor
CDS	Correlated Double Sampling
DAC	Digital-to-Analog Converter
DNL	Differential Non-Linearity
DFF	D Flip-Flop
ENOB	Effective Number of Bits
FPB	Fixed Pattern Noise
GUI	Graphic User Interface
INL	Integrated Non-Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
PD	Photodiode
PPS	Passive Pixel Sensor
SAR	Successive Approximation Register
SoC	System-on-Chip
SNR	Signal-to-Noise Ratio
SINAD	Signal to Noise and Distortion
SRAM	Static Random Access Memory
THD	Total Harmonic Distortion
VLSI	Very Large Scale Integration

Chapter 1

Introduction and Background

1.1 Background

Imagers are required to have an increasingly high number of pixels in order to keep up with consumer according demand. One consequence of this is that the bandwidth of readout circuitry needs to be significantly increased in order to read out all the pixels within the same frame time, and column-parallel analog-to-digital converter (ADC) architectures have therefore become more popular [3, 4, 8, 16, 21–23]. This type of architecture employs a large number of parallel ADC channels to facilitate the high-speed readout of large pixel arrays, and also integrates the system-on-chip (SoC) applications, especially in portable devices. Even so, the expansion of the mobile market relentlessly driving design technologies towards higher performance with lower power consumption.

In a CMOS image sensor system as shown in Figure 1.1,the red blocks are analog blocks, and the blue blocks are the digital blocks, which are normally powered up by different power supplies. Digital circuits are usually powered with lower supply voltages than analog circuitry, to achieve lower power consumption. The power consumption for an image sensor with intermediate resolution is mainly accounted for by analog circuits, where the current in pixel arrays is normally less than 1mA for roller shutter image sensors, and the column-level analog circuitry (correlated double sampling (CDS) circuit

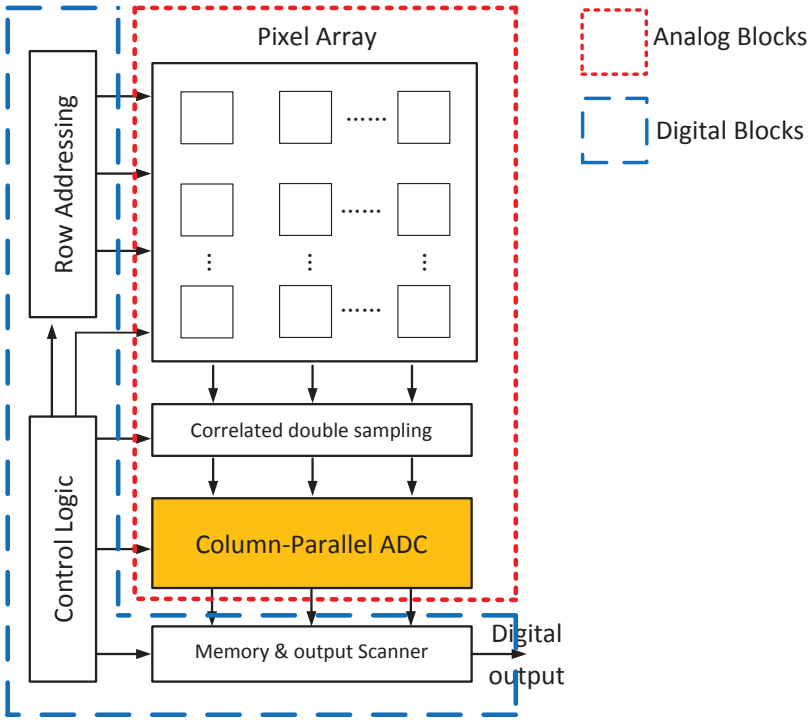


Figure 1.1: Overview of CMOS image senor architecture

and column-parallel ADC) is the block which consumes the most power. In the column-level circuitry, the ADC inevitably consumes more power than CDS, as is required in higher complexity circuit blocks. The column-parallel ADC system therefore plays an extremely important role in the total power consumption of an imaging system, and a low-power ADC solution is crucial for a low-power CMOS image sensor.

The column-parallel ADC architecture currently applied in CMOS image sensors is usually one of the following types: single-slope (SS) ADCs, cyclic ADCs, successive approximation register (SAR) ADCs and delta-sigma ($\Delta\Sigma$) ADCs. The SS ADCs are the most widely used in image sensors, as they can be implemented with a single comparator and ramp generator and it is relatively easy to ensure uniformity. A very high-speed clock is required in SS ADCs to guarantee the sampling speed, as the number of conversion steps for a N-bit SS ADC is 2^N [21] [22]. SAR ADCs are normally used for low-power applications due to their inherently low-power consumption with moderate sampling rate

and resolution. But the high resolution capacitive digital-to-analog converter (DAC) normally required at column level, consumes large silicon area and is unacceptable for some applications with a fine pixel pitch [4,16,23]. Cyclic ADCs are normally utilized for high-speed image sensors. They consume less silicon area consuming than SAR ADCs, but require highly accurate amplifiers at column level resulting in higher power consumption than SAR and SS ADCs. Regarding $\Delta\Sigma$ ADCs, the $\Delta\Sigma$ modulator is the core which produces the bitstream and low pass filter. This type of ADC is mainly comprised by the logic circuit blocks and its performance is limited by the $\Delta\Sigma$ modulator [3] [17]. $\Delta\Sigma$ ADCs therefore have the simplest circuitry but their most operating algorithm comparing is more complex than that SS ADCs, SAR ADCs and cyclic ADCs.

Considering the above mentioned differences between column-parallel ADC architectures, it can be seen that SS ADCs are more suitable for CMOS image sensors with an extremely small pixel pitch, but with moderate speed, resolution and power consumption. $\Delta\Sigma$ ADCs consume less silicon array compared to the others, but their layout is not well suited to a small pixel pitch, making them more widely used in low-speed CMOS image sensors with low-power and low-silicon consumption requirements. SAR ADCs and cyclic ADCs are more suitable for high-resolution applications, with cyclic ADCs being more suitable for high-speed application, while SAR ADCs are used more in CMOS image sensors with low-power solutions. The most suitable architecture for low-power applications with relatively high resolution and speed is therefore that of SAR ADCs. In this study we also looked at innovative architectures for reducing the size and power consumption of the capacitive DAC in SAR ADCs.

1.2 Motivation and Objective

Figure 1.2 shows a general CMOS imaging system. The blocks inside are illustrated based on function distribution. The pixel array are used to perform photon-to-electron

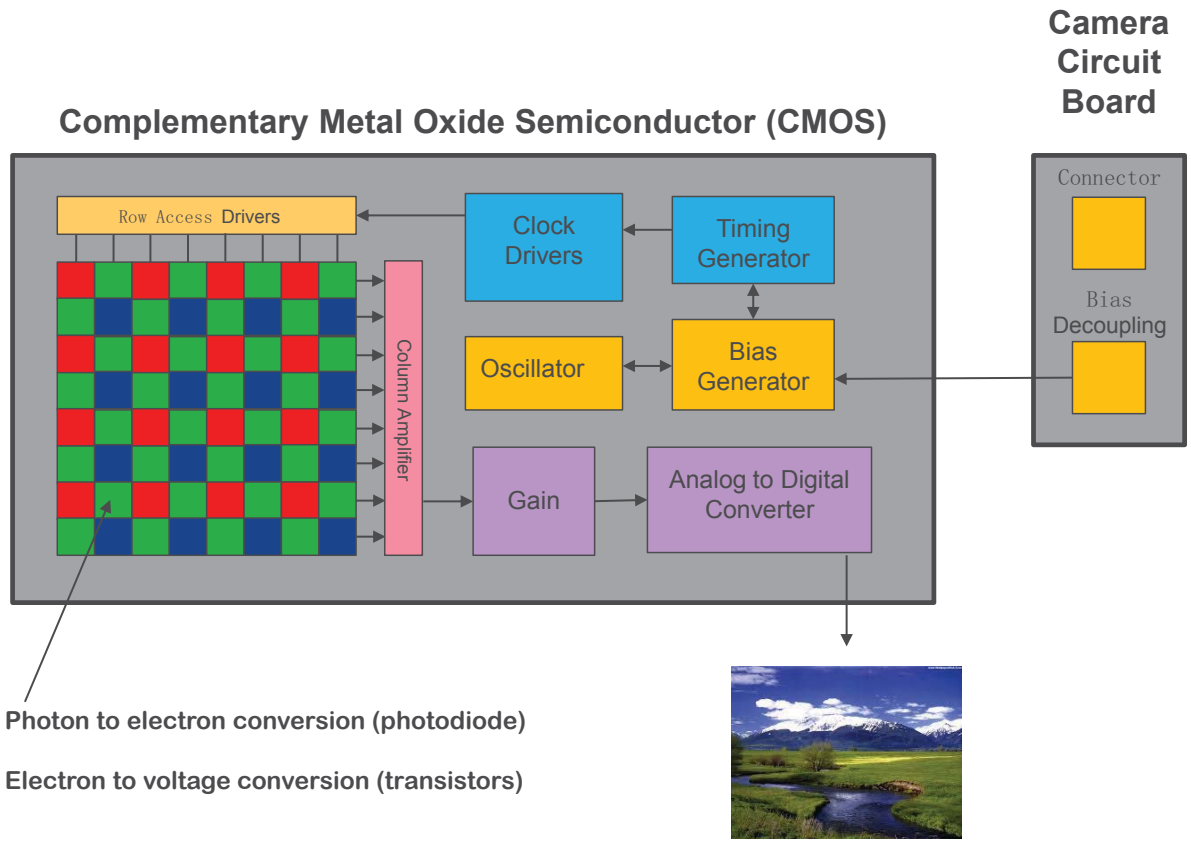


Figure 1.2: Overview of a CMOS imaging system

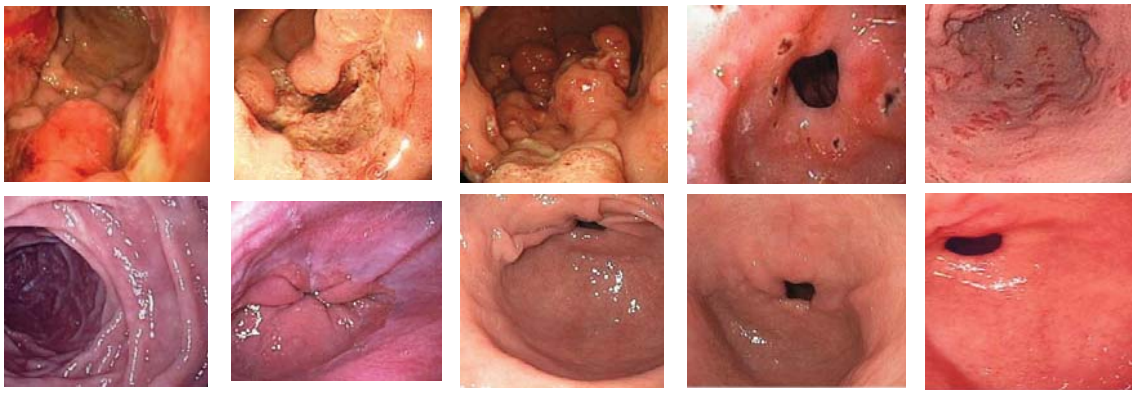
conversion (photodiode) and electron-to-voltage conversion (transistor), and the voltage is applied to the ADC after amplification. The quantization results of the pixel outputs (analog inputs to ADC) are later read out and calculated to form an image. In fact, the imaging system can be classified as a system-on-chip (SoC) application for the large amount of analog input signal processing that needs to be carried out inside it. Those analog input signals captured by an image sensor from real world would have inherent correlation, resulting that various innovations and operating algorithms based on the imaging system are proposed.

Take reference [5] for example, which shows a CMOS image sensor with on-chip image compression is illustrated. Image compression is usually performed off-chip because it is both time and energy consuming. The proposed design incorporates an adaptive on-

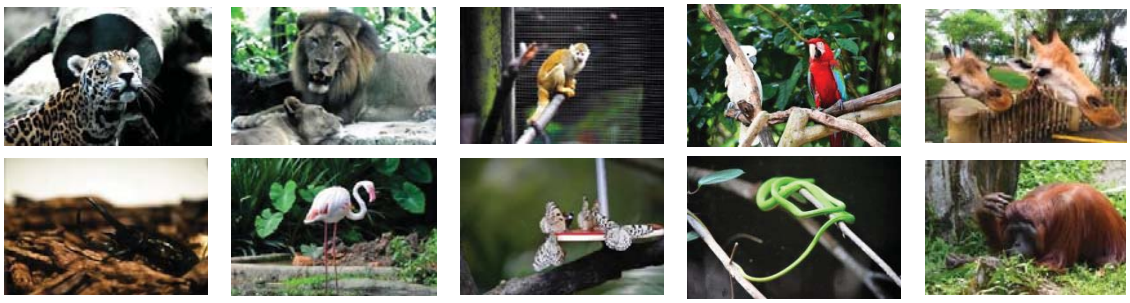
chip quantization scheme based on a memoryless quadrant tree decomposition (QTD) algorithm and the predictive fast boundary adaption rule. This system-level innovation is based more on the values of the imaging data and the correlation which exist between them. The low-power solution for column-parallel ADCs in CMOS image sensors is therefore implemented in two places: in imaging system itself, with its large amount of data; and in the ADC architecture, which is used for quantizing the analog input to digital data as discussed in the previous section.

A similar approach, considering both ADC architecture and analog inputs, has also been studied in biomedical applications [14]. As the input signal movement trend in biomedical applications is known or predictable, an innovated design is also proposed for SAR ADC architecture, changing the successive approximation search algorithm to match the historical data changing trend. In order to achieve a low power biomedical data acquisition system with exploring the architecture of SAR ADCs only.

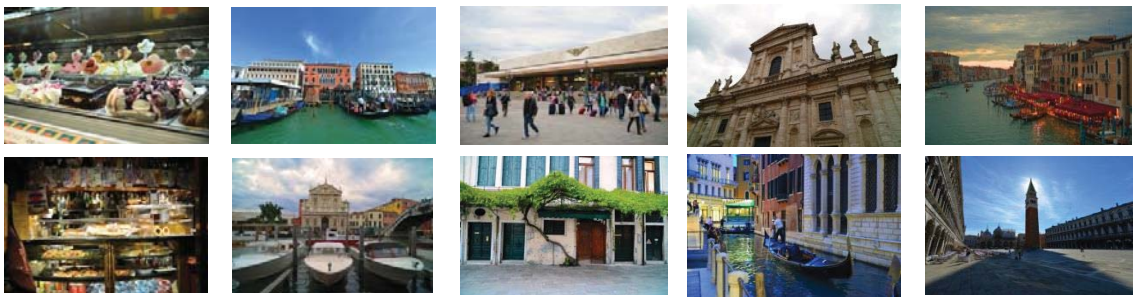
Just as different types of CMOS image sensor applications vary widely, the images they capture also have different properties. In capsule endoscopy, the images captured show the inner part of the stomach as shown in Figure 1.3(a), where the pixel values of them are almost same. Mobile cameras are mainly used to capture natural scenes, which also have high similarity values because of their low complexity. In Figure 1.3 (b) and (c), showing two groups of pictures taken at Singapore zoo and in Venice, Italy, some portions of the images are occupied by the same objects, or the same background (for example sky, water, buildings, trees, the skin of animals, etc). Figure 1.3(d) shows some sample photos taken from internet, which are standard images for image processing. In those images, high spatial likelihood exists in natural scene or in the values of nearby pixels. In CMOS image sensor hardware, the analog signal in a pixel array is quantized row by row to a digital signal by column-parallel ADCs: each ADC charges one column of pixels, which is later read out to form an image. with this combination of operating



(a) Inner views of stomach and intestine.



(b) Pictures taken at Signapoe Zoo.



(c) Pictures taken at Venice, Italy.

Figure 1.3: Sample images of stomach and natural scenes.

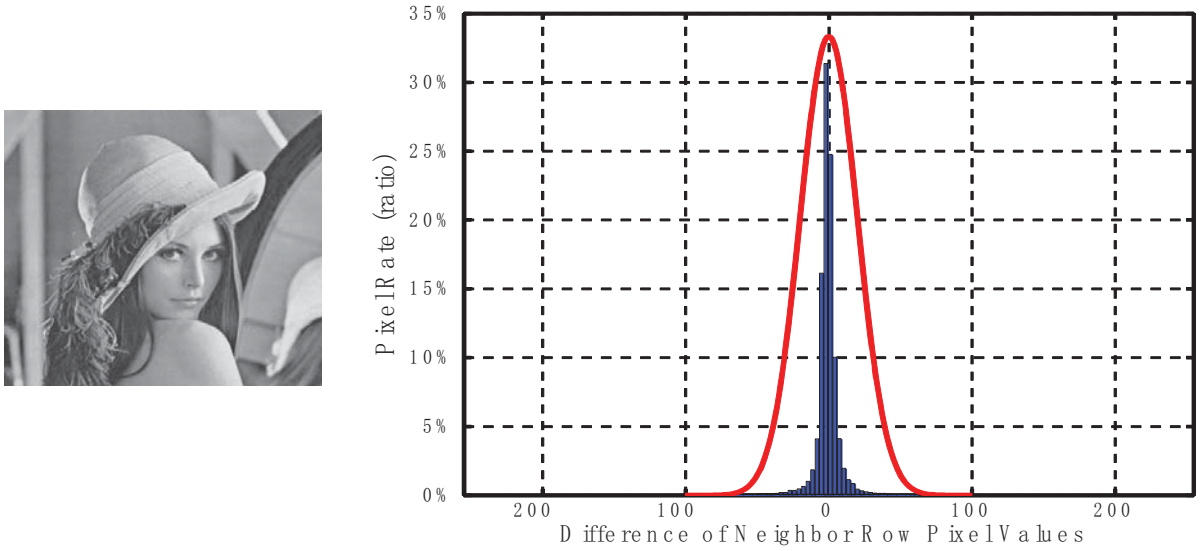


Figure 1.4: Distribution diagram of neighbor-row-pixel difference values (Δ) in an image (Lena 512 $\times$ 512). Δ is mainly located within a range of -50 to 50 with a pixel value range of [0,255].

procedures, strong correlation can be observed between consecutive rows in most natural scenes.

To corroborate this phenomenon, a MATLAB simulation of the sample images was performed to calculate the distribution density for difference between neighbor-row pixels. The simulation results showed strong correlation between consecutive rows of images, with most of the difference being small in value and distributed around zero. Take the distribution curve of a 512×512 resolution Lena image for example, as shown in Figure 1.4, the distribution diagram for neighbor-row-pixel differences in the Lena image is shown by a blue bar, and the red curve is the Gaussian envelop curve. It can be seen how the difference values are distributed in concordance with the properties of the Gaussian curve, mainly around 0, within a range of [-50, 50] for a maximum pixel value of 255.

In a general CMOS image sensor, the same ADC operation is repeated column to column, row to row and frame to frame, regardless of the properties of the scene. In this proposed design, however, neighbor pixels can be used to estimate the value of a selected

pixel, exploiting the likelihood of natural images to narrow down the difference between the reference voltage and the analog input. The smaller the difference, the fewer the A/D conversion cycles needed for the same resolution, and the lower the power required in the ADC system. The main motivation for this project was to achieve a low-power column-level ADC system solution by reducing the A/D conversion of similar pixels.

This design proposes a prediction scheme for column-parallel ADCs based on the properties mentioned above. The objectives of the study were (i) to develop a new design methodology which takes these properties into account for natural scenes, (ii) to implement this idea in an image sensor with adaptable ADC architecture: successive approximation register (SAR) ADC was chosen, because this type of ADC usually contribute to low power solutions in ADC design and its operating algorithm is more adaptable for the proposed methodology; (iii) to design the schematic and layout of an image sensor chip with the proposed ADC architecture using AMS 0.35μm CMOS technology, and to test it using an FPGA system; and (iv) to perfect the proposed algorithm and the hardware associated with the design and testing of the prototype CMOS image sensor.

1.3 Thesis Organization

The rest of this thesis consists of three chapters. Chapter 2 presents a background study and a review of literature about CMOS image sensors, illustrating the constitution and operation principle of such sensors. Chapter 3 describes the basic architectures of column-parallel ADCs applied in CMOS image sensors, and their performance metrics. Chapter 4 illustrates the design details of a low-power column-parallel ADC for use in CMOS image sensor based on the spatial likelihood of natural scenes. The high similarity characteristics of neighbor pixels from groups of sample images are first analysed and a prediction scheme based on that analysis is then proposed and explained. At the end

of chapter 4, the VLSI hardware design for this algorithm is illustrated step by step, together with the hardware testing. Chapter 5 describes an updated version of the design with several improvements to the algorithm and the hardware architecture, and discusses the calibration of column-parallel ADCs. It also describes a new procedure flow for the prediction scheme and the corresponding changes in the hardware architecture. The last chapter presents the main conclusion of this project, and the benefits of this master program.

Chapter 2

Introduction to CMOS Image Sensor

2.1 Image Signal Chain and Overall Architecture

An image sensor is a device that converts an optical image into an electronic signal, and mostly utilized in digital cameras, camera modules and other imaging devices [2, 7, 9, 19, 25]. The optical image represent the number of incident photons, and the electronic signal is the digital signal that quantizes the number of the incident photons. The image signal chain from initial photon to final digital signal is illustrated in Figure 2.1. Initially, the incident photons are assigned in the photo-detector, and this device transfers the photons into electrons. This generated electrons are swept by the electric field, which is built by the reverse-biased voltage applied to the photo-detector. Therefore, the photocurrent (i_{ph}) is formed in this photo-detector , and later it is converted into voltage signal (V_{PD}) through the integration of photocurrent as shown in Figure 2.1(b). This analog voltage signal will be read out though the in-pixel amplification circuits, and be quantized into digital signal through the analog-digital converter (ADC), as the digital signal are used to generate the corresponding optical image into a digital image.

In terms of a CMOS image sensor architecture as shown in Figure 2.2, it is consisted by the pixel array , correlated double sampling (CDS) circuitry, column-parallel ADCs, memory and row/column scanners, which is popular architecture widely used nowadays. The pixel array is the core component of an image sensor as it is the image capturing

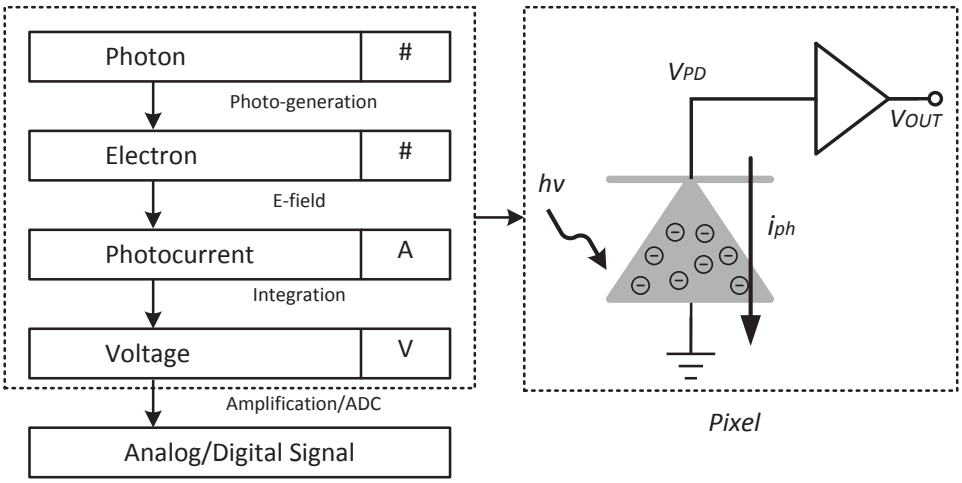


Figure 2.1: The procedure of image signal.

region, and the number of pixels determine the resolution of an image The CDS are not utilized in every image sensor, as it is not compile with 3T active pixel sensor (APS) (which will be discuss in Section 2.4).

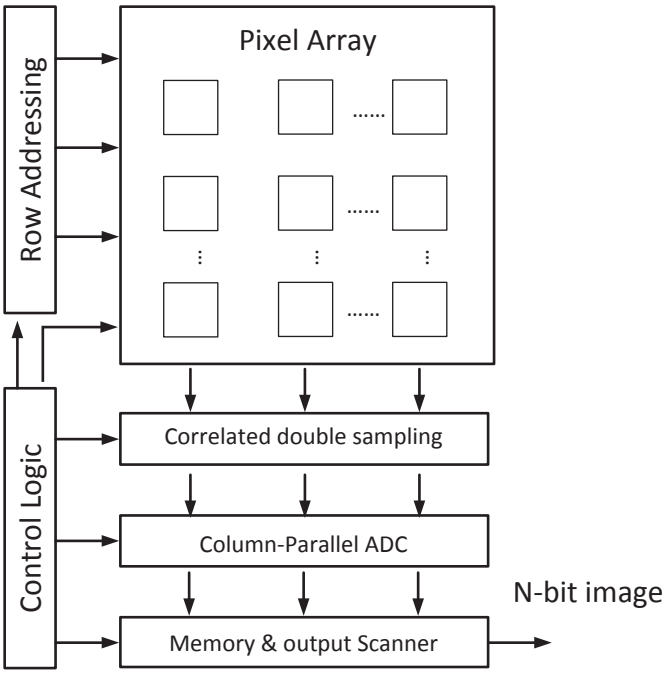


Figure 2.2: Overall architecture of a CMOS image sensor.

The operation procedure of this image sensor can be illustrated as follows: (1) The incident photons from the optical image is converted to electronic signal through the photodiode in the pixel array, and the integrating time (T_{int}, also called exposure time) is required to accumulate the electrons in photodiode in each pixel. The exposure time determines the amount of the incident photons collected and accumulated into electrons, and the final digital image will be too bright if exposure time is too long, or too dard vise verse. (2) The in-pixel circuit converts the electron accumulated in photodiode to voltage signal, and each pixel has one analog output. (3)Then the row scanner scans the pixel array row by row, so the pixel signals of one row are sent to column-level circuits (CDS, ADC and memory). (4) The CDS is used to cancel the noise at reset mode during the pixel operation. (5) The clean analog pixel values are sent to ADCs for quantization, and those digital signals for one row pixels are temporarily stored into the memory after A/D conversion. (6) Those stored digital signals are scanned outside for reading column by column through the column scanner.(7) The above procedures are repeated for next row until the entire rows are finished, and one image frame can be generated.

2.2 Photogeneration

As discussed in above section, the photon generation is core procedure for the imaging system, as the photon represents the optical image information. The photon is the carrier of electromagnetic radiation of all wavelengths, which is traveling at the speed of light and the energy of the photon is expressed as Equation Eq. 2.1.

$$E = h\nu = \frac{hc}{\lambda} \tag{Eq. 2.1}$$

where h is Planck's constant, c is light speed, ν is the frequency, and λ is the wavelength.

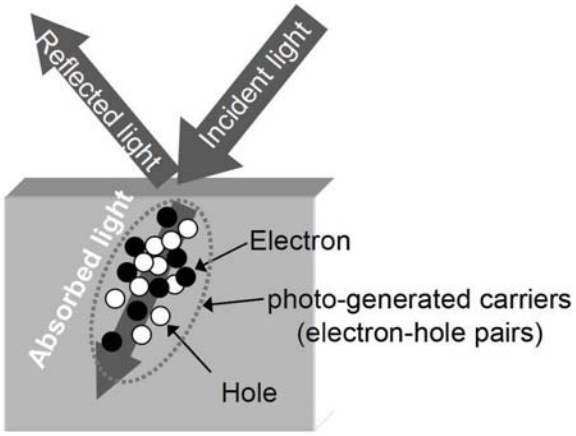


Figure 2.3: Photo-generated carriers in a semiconductor with incident light applied.(Ref [19]Chapter 2)

For photodetectors, the silicon is the most widely used material, which is also used for CMOS circuits. For the incident light on a semiconductor(silicon), normally only part of the light is absorbed and the rest is reflected. The absorbed light can produce electron-hole (e-h) pairs inside semiconductor, which are called photo-generated carriers, as shown in Figure 2.3. The amount of photo-generated carriers is described by the absorption coefficient α, which is described as follow.

$$\alpha(\lambda) = \frac{1}{\Delta z}\frac{\Delta P}{P} \qquad \text{(Eq. 2.2)}$$

where Δz is a distance traveled by the light, and ΔP/P is the ration of decrease of light power.

Regarding the silicon material, the energy band diagram is defined in Figure 2.4, and the bandgap energy (E_g) is the energy for a free electron travel from valence band into conduction band. When the photon energy exceeds the E_g of silicon, one electron moves to the conduction band and corresponding hole is generated at valence band. As a result, one e-h pair is created as shown in Figure 2.4(a) , and this process is called photogeneration. When the excited electron meets the hole in the valence band and

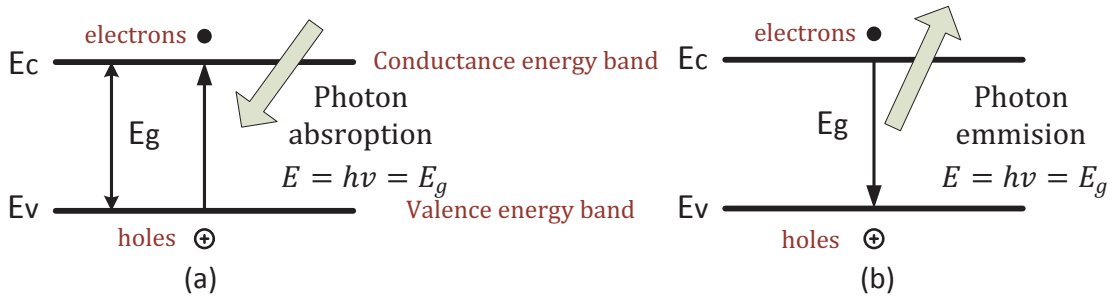


Figure 2.4: Energy band diagram of (a) Absorption, (b) Recombination.

occupies that place as illustrated in Figure 2.4(b). As a result the e-h pair will disappear, and the electron energy is released as a photon with energy closed to the E_g. This process is called recombination.

In the absence of illumination, the electron and hole concentrations in the conduction and valence band are defined as n_0 and p_0 (where $n_0 = p_0$). The Δn and Δp are the additional concentrations generated by the light, and the new electron and hole concentrations are defined as:

$$n = \Delta n + n_0$$
$$p = \Delta p + p_0 \qquad \text{(Eq. 2.3)}$$

As mentioned in Section 2.1, those generated electron signals will be transferred to photocurrent and later be converted to voltage signals which can be processed and readout by following circuitry.

2.3 Photodetector

A photodetector is an optoelectronic device that absorbs optical energy and converts it to electrical energy, which usually manifests as photocurrent. Since the photo-generated electrons are generated in the semiconductor, as well as lost during the recombination. So the material used for photogeneration should be designed to minimized the loss of

electrons, in order to reach a detectable signal level during a certain integration time. Thus, the p-n junction photodiodes (PDs) are most used in CMOS image sensors, since the electric field generated in p-n junction can prevent the moving of electrons from conduction band to valence band.

2.3.1 P-N Junction Phototdiode

The p-n junction photodiode is a type of photodetector which is available from the standard CMOS process. The architecture and voltage potential diagram of a p-n junction without illumination is presented in Figure 2.5. The p-n junction photodiode is consisted by a p-type and a n-type silicon, and the gray portion in middle is the depletion region formed by the potential difference (V_0). The potential barrier V_0 blocks the electrons in the n-type region from diffusing into p-type, as well as the holes in p-type region from diffusing into n-region. Thus, there is no electron moving between both regions, as a result there is no current flow in this diode.

When this junction is under illumination, it is equivalent to the operation of a diode with reverse bias applied ($V = -V_r$). As shown in Figure 2.6, those e-h pairs generated move in the same directions as the minority carriers in the reverse biased junction (in the darkness). As a result, the potential barrier is enlarged by value V_r and a photocurrent is generated by the moving of e-h pairs.

2.3.1.1 Photocurrent

Since the photocurrent is generated by the movement of e-h pairs accumulated through the light illumination, so the photocurrent is consisted by the moving of e-h pairs in different regions in p-n junction diode. As show in Figure 2.7, the internal E-field (formed by $V = -V_r$ as shown Figure 2.6) sweeps the photogenerated electron to the n-side and the photogenerated hole to the p-side in the depletion region. It results a drift current that flows in the reverse direction from the n-side to the p-side. At the edges

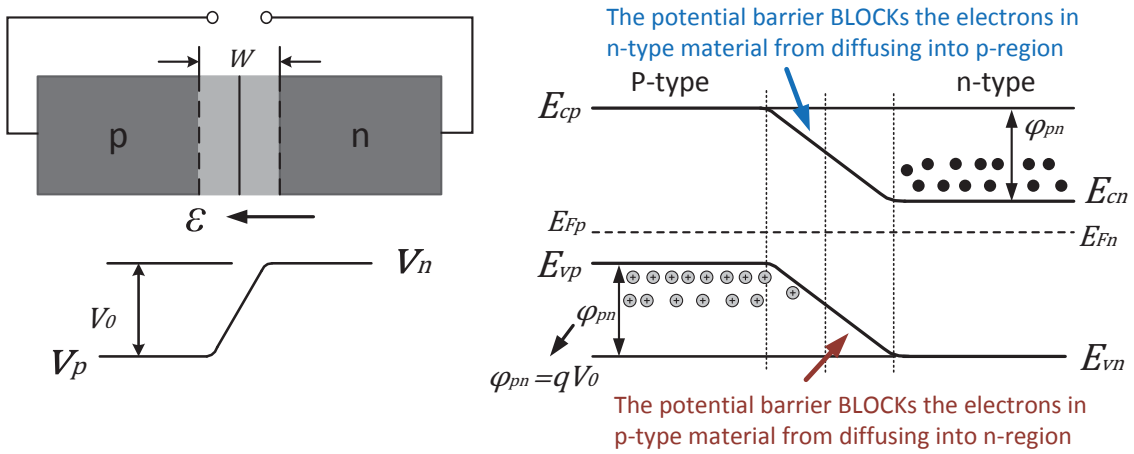


Figure 2.5: P-N junction photodiode.

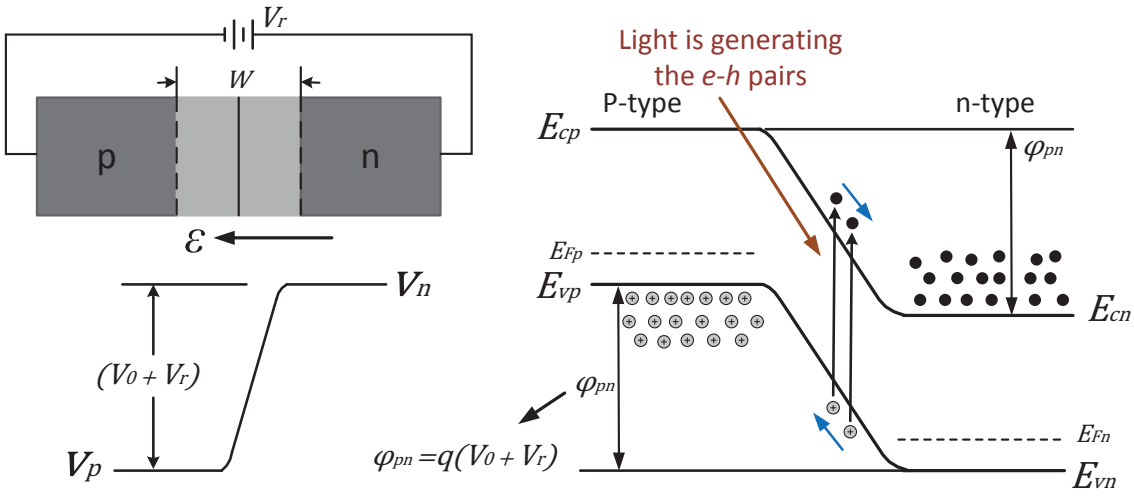


Figure 2.6: P-N junction photodiode with light illumination.

of the depletion layer (diffusion regions), the photogenerated minority carrier (holes in the n-side and electrons in the p-side) can reach the depletion region by diffusion and then be swept to the other side by the internal E-field. As a result, a diffusion current is generated with the same reverse direction as drift current. In the p or n homogeneous region, there is no internal filed to separate the charges, so there is essentially no current is generated. Therefore, the resulting junction photocurrent from n-side to p-side can be expressed as:

$$I_p = eA(L_n + L_p + W)G \approx eAWG \qquad \text{(Eq. 2.4)}$$

where G is the photogeneration rate that gives rise to a photocurrent, and the A is the cross section area of the junction that is assumed to be uniformly illuminated by the photons with $h\nu > E_g$. Regarding Eq. 2.4, the AL_nG and AL_pG are the numbers of holes and electrons created per second within a diffusion length L_h and L_e on the n-side and p-side respectively. The AWG carriers are generated within the depletion region with width W. Since the depletion width W is much larger than diffusion length (L_n and L_p), so the photocurrent is mainly contributed by the drift current generated at depletion region.

2.3.1.2 Dark Current

The dark current is defined as a leakage current of a photodiode without any illumination, and it's value is typically dependent on the process [12]. The dark current in PDs has several sources, which can be mainly categorized by two: reverse-bias leakage and the surface generation current [15, 18]. The dark current mechanism is illustrated in Figure 2.8, the reverse bias leakage is mainly consisted by two components: (1) generation-recombination (g-r) current in the depletion region caused by thermal generation; (2)minority carriers diffusion current. The surface generation current is mainly

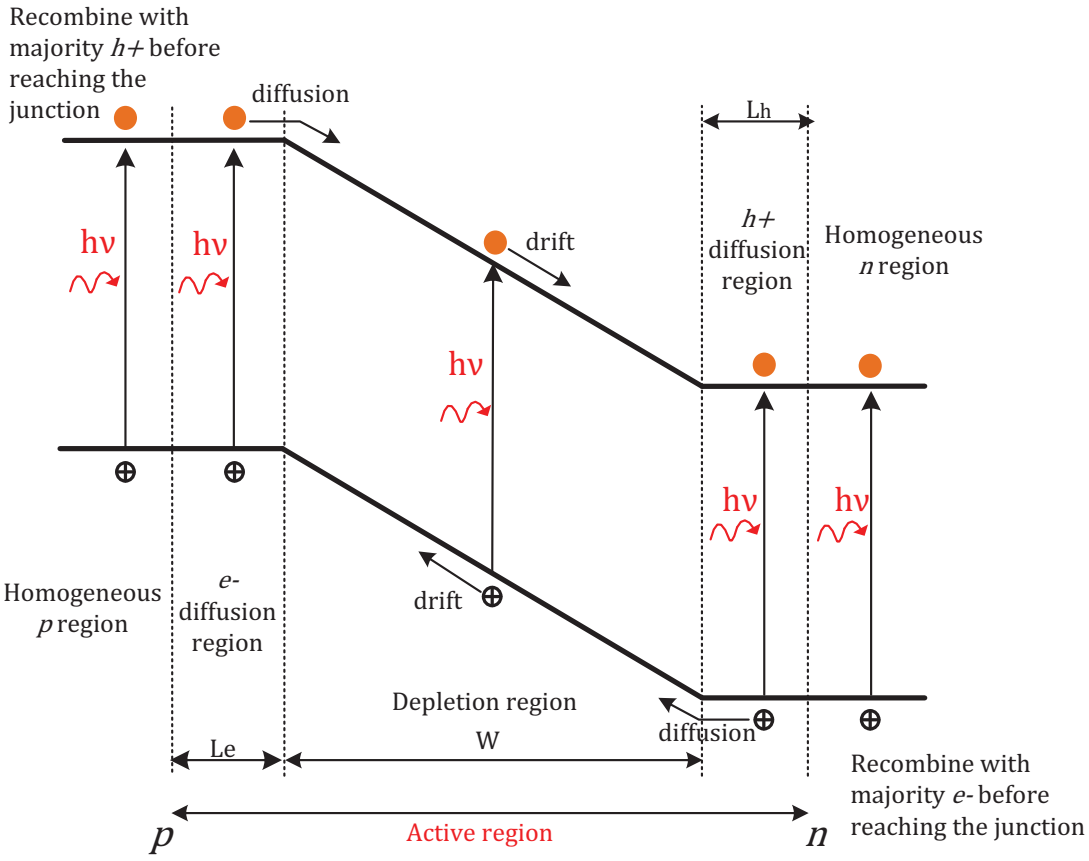


Figure 2.7: Photo-excitation and energy-band diagram of a p-n photodiode.

generated at (1) the surface of n-region and (2) the interface with STI. Therefore, the dark current can be expressed as follow:

$$\text{g-r current: } J_{g-r} = q\frac{n_i}{\tau_G}W \tag{Eq. 2.5}$$

$$\text{Diffusion current: } J_{DIFF} = q\sqrt{\frac{D_n}{\tau_n}\frac{(n_i)^2}{N_A}}W \tag{Eq. 2.6}$$

$$\text{Surface generation current: } J_{SG} = \frac{qG_S}{2} \tag{Eq. 2.7}$$

$$\text{Total dark current: } J_{DARK} = J_G + J_{DIFF} + J_{SG} \tag{Eq. 2.8}$$

where n_i is the intrinsic concentration of silicon, τ_G is the generation lifetime ($\tau_G = \tau_n + \tau_p$), W is the depletion width, G_S is the surface generation rate. The intrinsic concentration n_i and depletion width W are expressed as follow:

$$n_i = \sqrt{N_C N_V e^{-E_g/(2KT)}} = A(\frac{T}{300})^{3/2}e^{-E_g/(2KT)} \tag{Eq. 2.9}$$

$$W = \sqrt{\frac{2\epsilon(N_A + N_D)(V_{bi} - V)}{qN_A N_D}} \tag{Eq. 2.10}$$

where N_C, N_V are the carriers densities, E_g is the bandgap energy, N_A and N_D are doping concentrations, and V_{bi} is the built-on potential of the p-n junction.

According to Eq. 2.5Eq. 2.6Eq. 2.7Eq. 2.8, the factor affecting the dark current can be categorized by three: (1) Temperature: the higher the temperature, the higher the n_i, as a result of higher dark current. (2) Doping concentration: the higher the doping concentration, the higher τ_G, so the dark current increases. (3) Reverse bias voltage: the dark current increases due to increased W caused by the higher reverse-biased voltage.

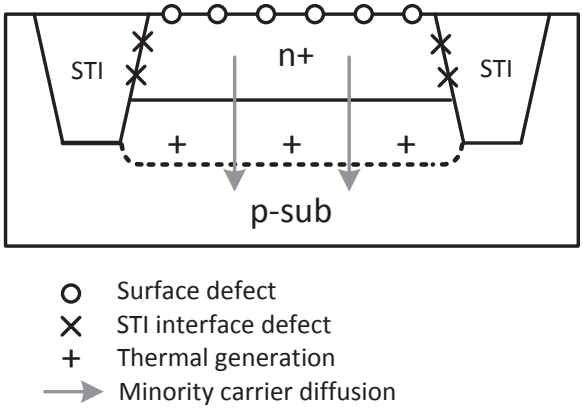


Figure 2.8: Mechanism of dark current.

The dark current of a p-n photodiode causes the shot noise and fixed pattern noise, which could decrease the signal-to-noise (SNR) performance. Thus, the process with suppressed dark current is good choice for CMOS image sensor design.

2.3.1.3 Charge Integration and Detection

Since the photodiode is equivalent to a capacitor with junction capacitance, so the photocurrent (I_{ph}) is integrated in this capacitor as well as the dark current. As shown in Figure 2.9, the operation procedures is illustrated. (1) The photodiode is reset to V_R before the integration of photocurrent ($V_{PD} = V_R$); (2)later photocurrent discharges the junction capacitance (C_D) during the integration time given (T_{INT}); (3)After T_{INT}, the value of V_{PD} node is read out by following circuitry; (4) the PD is reset again and a new frame starts. The decrease amount of the V_{PD} is the voltage accumulated from the photons absorbed.

2.3.1.4 Full Well Capacity

The full well capacity can be equivalent to the maximum capacity of a bottle, where the photodiode is described as the bottle. In a word. the full well capacity defines the amount of charge an individual pixel can hold before saturating, and it can be calculated as following:

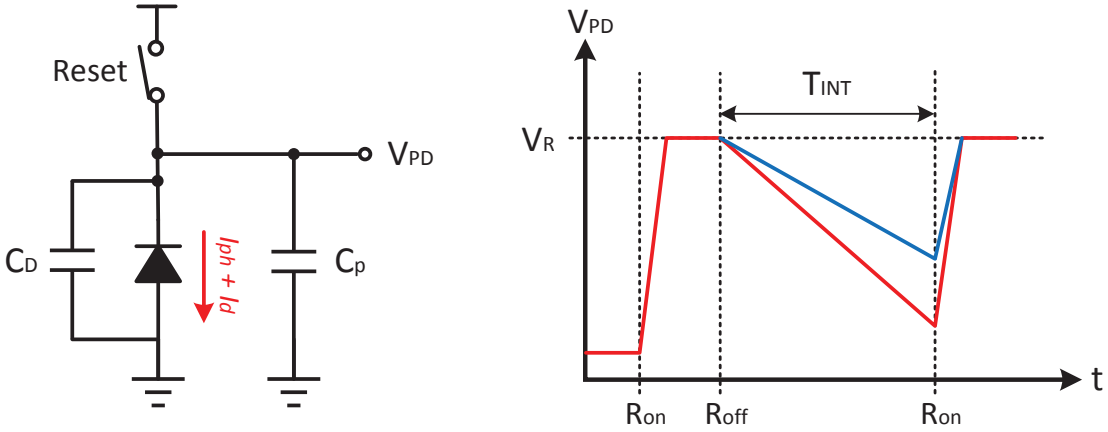


Figure 2.9: Charge integration of a photodiode.

$$
\begin{aligned}
N_{sat} &= \frac{1}{q}\int_{V_{Reset}}^{V_{Reset}-V_{Swing}} C_{PD}(V)dV \text{ [electrons]} \\
C_{PD}(V) \approx C_j &= A_{PD}\left(\frac{q\epsilon N_D N_A}{2(N_D+N_A)(V_{bi}-V)}\right)^{\frac{1}{2}} \text{ for p-n junction} \\
&\approx A_{PD}\left(\frac{q\epsilon N_A}{2(Vbi-V)}\right)^{\frac{1}{2}} \text{ for p-n+ junction}
\end{aligned}
\qquad \text{(Eq. 2.11)}
$$

where C_{PD} and C_j are the capacitance of PD and junction respectively, V_{Reset} and $VSwing$ are the reset and maximum swing voltage of PD. The full well capacity can be expressed as following, if the C_{PD} is assumed to be constant,

$$
\begin{aligned}
N_{Sat} &= \frac{C_{PD}V_{Swing}}{q} \text{ [electrons]} \\
Q_{Sat} &= C_{PD}V_{Swing} \text{ [C]}
\end{aligned}
\qquad \text{(Eq. 2.12)}
$$

2.3.1.5 Conversion Gain

The amount of voltage vary from one electron is the conversion gain of a PD, which is expressed as following:

$$A_C = \frac{q}{\text{Capacitance of dectection node}} = \frac{q}{C_{PD}} \ [\mu \text{ V/electron}] \quad \text{(Eq. 2.13)}$$

Thus, the higher the conversion gain, the higher voltage swing of the PD; since the voltage converted by same amount of photons absorbed is higher. In p-n junction PD, the capacitance of detection node is C_{PD}, and the C_{PD} should keep smaller to have higher conversion gain with purpose of higher voltage swing and sensitivity.

2.3.1.6 Sensitivity

The sensitivity is defined as the ratio of output signal [V] to an incident illumination level [lx] in a second. The unit of sensitivity is [V/lxs]. Note that high conversion gain increase the sensitivity, however, high sensitivity does not guarantee that the pixel has high conversion gain. The sensitivity can be increased from process optimization, microlens optimization, and so on.

2.3.1.7 Fill Factor

Normally, one pixel is formed by the PD and in-pixel readout circuits (typically source follower), and not the whole pixel area is applicable for light detection. The fill factor (FF) is used to describe the ration of light sensitive area (PD) versus the total area of a pixel. The FF can be expressed as Eq. 2.14

$$FF = \frac{A_{PD}}{A_{PIX}} \ [\%] \quad \text{(Eq. 2.14)}$$

Since larger fill factor means the large silicon area to collect the light photons, so the sensitivity of a PD is higher. In case the fill factor is too small, the fill factor usually is improved by the addition of micro lenses, where the lens collects the light impinging onto the pixel and focuses the light to the light sensitive area of the pixel. Another way

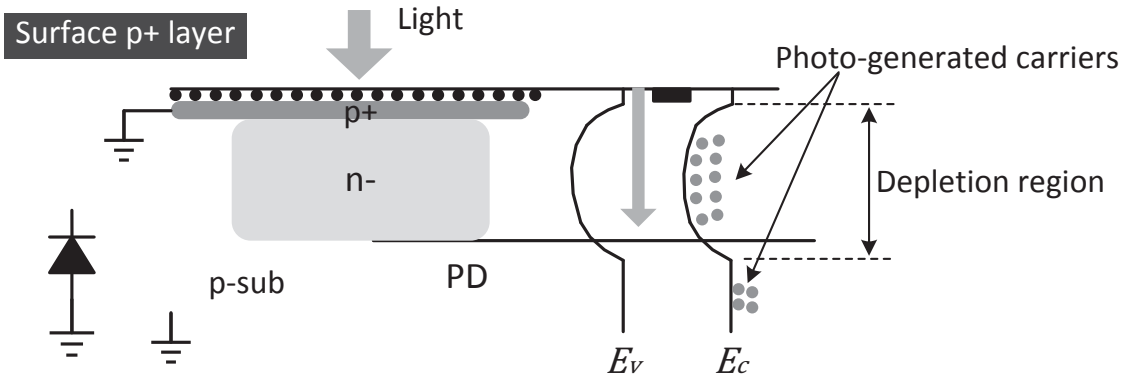


Figure 2.10: Behavior of photo-generated carriers in a pinned photodiode (PPD).

to improve the FF during designing is backside illumination (BSI) technology, where the PDs are exposed to the backside and the metal lines are located in the front side.

2.3.2 Pinned Phototdiode

The structure of pinned photodiode (PPD) is shown in Figure 2.10, the topmost surface of the PPD has a thin p^+ layer and the p-n junction PD is buried under this surface. This addition p^+ layer has the same potential as the p-substrate region, and the potential profile at the surface is strongly bent. Thus, it isolates the accumulation region (p-n junction PD) from the surface.

Therefore, the photo-generated carriers generated at shorter wavelength are quickly swept to the accumulation region by the bent potential near the surface and contribute to the signal charge. This architecture has few improvements comparing a conventional PD:(1) The dark current of this architecture is less,as the pinned layer masks the surface current which is main source of dark current. (2)The large bent potential in the surface produces an accumulation region with complete depletion, where the collected photons can be accumulated into the PD well and completely transfer to the sense node for pixel readout. The structure of PPDs important for 4-T type active pixel sensors, and it has been used for CMOS image sensors with high sensitivity recently.

2.4 Basic Pixel Architecture

The basic pixel architecture is consisted by a phtotodetector, together with accessing and readout circuits, which has different architecture applied in CMOS image sensor. Historically, passive pixel sensors (PPS) were developed first, in which the photodiode is simply connected with a transistor switch for pixel access. Then active pixel sensors (APS) were developed to improve image quality, which is popularly used in imaging applications nowadays. The APS has three transistors connected with photodiode to form a pixel, which is called 3T-APS. The so-called 4T-APS had one extra transistor inside a pixel comparing with 3T-APS, which has greatly improved the image quality, but request more complicated fabrication process [2, 19, 25]. The details of both APS are discussed in the following sections respectively.

2.4.1 3T APS, PN Junction PD

As shown in Figure 2.11, this APS is named after its active element which amplifies the signal in each pixel. The pixel configuration of this 3T APS is consisted by a photodiode (PD), a reset transistor (M_{RST}) , a source follower transistor (M_{SF}) and a row select transistor (M_{RSL}). The signal is transferred to a vertical output line through the select transistor(M_{RSL}, and the column output bus is share for all rows in this column. The control signals (RST, SEL) are driven by the row scanner, and the timing diagram of both signal is shown in Figure 2.12.

The operation of the 3T APS is described as follows: (1) Reset:the photodiode (PD) is reset to the value $V_{dd} - V_{th}$, where V_{th} is the threshold voltage of transistor M_{RST} as shown in Figure 2.11. It is obtained by turning on the reset transistor M_{RST}.(2) Integration(Exposure):the transistor M_{RST} is turned off, and the photo-generated carriers accumulated in the PD junction capacitance C_{PD} when light is incident. Then the accumulated carriers changes the potential in the PD, and the voltage of the PD V_{PD}

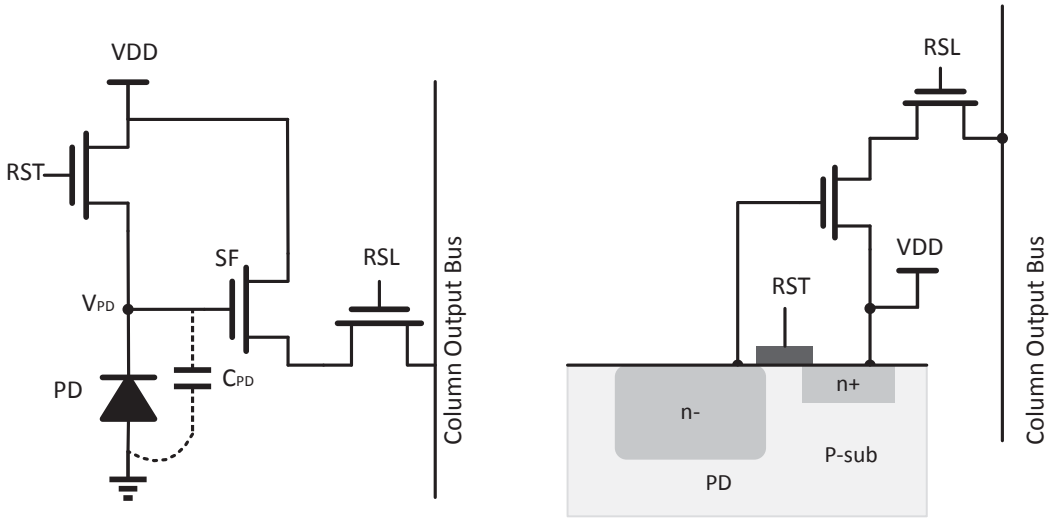


Figure 2.11: Basic pixel architecture of 3T-APS.

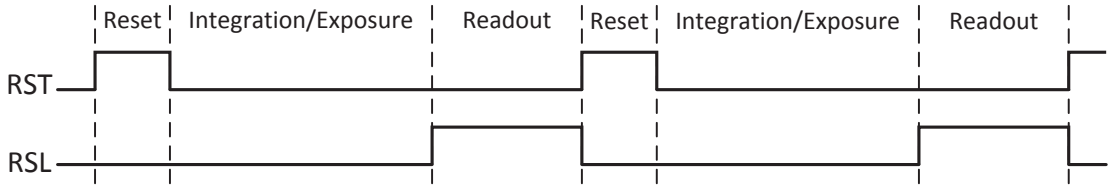


Figure 2.12: Timing diagram of 3T-APS.

decrease according to the input light intensity. (3) Signal readout: after an accumulation time, the select transistor M_{RSL} is turned on and the output signal in the pixel is read out in the vertical output bus which is connected to the column-level circuitry. (4) Reset: after the read-out process, the M_{RSL} is turned off again and M_{RST} is turned on to repeat the above process(1)(2)(3).

Even though the APS overcomes the drawbacks of PPS, and improve the image quality. There are some issues with 3T APS:

- The thermal noise is difficult to suppress;
- The PD design is constrained by the simultaneous work of the photodetection and photoconversion in photodectection region (PD).

2.4.2 4T APS, Pinned PD

Comparing with 3T APS, the 4T APS introduced a transfer gate (TG) and a floating diffusion (FD) to the 3T APS pixel architecture, and this transistor (M_{TG} is used to transfer the charge accumulated in the PD to the FD. This configuration is called 4T APS based on the total number of transistors in a pixel, and its schematic and cross-sectional view is shown in Figure 2.13.The control signals (RST, SEL, TG) are driven by the row scanner, and the timing diagram of both signal is shown in Figure 2.14.

The operation procedure is described as follow: (1) Reset: transistor M_{TG} and M_{RST} are both turned on, the PD is reset to the value $V_{dd} - V_{th}$, where $V_{dd} - V_{th}$ is the voltage of at node SF (V_{FD}) as shown in Figure 2.13. At the same time, the FD is also be reset. (2) Integration (Exposure): transistor M_{TG} is turned off, but M_{RST} is still be kept on, which separates the PD and FD with purpose to separate the photo detection region and photo conversion region. During this phase, the signal charge is accumulated in the PD, and the FD is keeping reset mode. (3) Readout reset signal: after accumulation

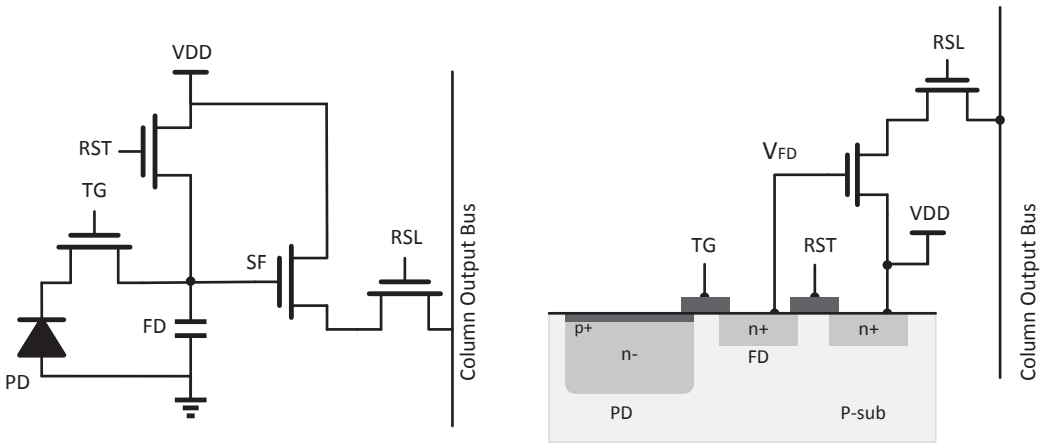


Figure 2.13: Basic pixel architecture of 4T-APS.

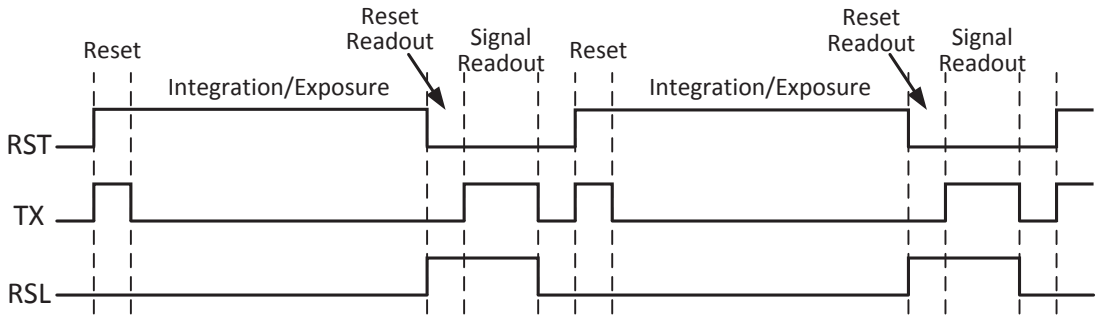


Figure 2.14: Timing diagram of 4T-APS.

of signal charge, and before transferring it out, the reset value at FD should be read out for correlated double sampling (CDS) by turning on the select transistor (M_{RSL}). (4) Readout PD signal: after the reset readout is finished, the transistor M_{TG} is turned on and the signal charge accumulated at the PD is transferred to the FD. Meanwhile, the M_{RSL} is still kept on for the following readout to column bus. (5) Reset: transistor M_{TG} and M_{RST} are both turned on again, and M_{RSL} is turned off. Repeating this above process, the reset charge and signal charge are read out.

In this 4T APS operation, the operating timing of those control signals do help on the separation between the charge accumulation region (PD) and the charge transfer, readout region (FD). It eliminates the thermal noise mentioned in 3T APS, and also enable the CDS operation for low noise sensor operation. Comparing to the P-N PD structure of 3T APS, the pinned PD is required for 4T APS, as the charge of PD should be drained completely in the readout process and pinned PD works better on this way.

Although the 4T APS has better performance than 3T APS in low noise application, there are some issues with 4T APS:

- The fill fact (FF) is reduced by the additional transistor (M_{TG}) comparing to 3T APS;
- If the accumulated signal charge is completely transferred into FD, the image lag might occur;
- The fabrication process parameters is tough to establish for the pinned PD, transfer gate, FD, reset transistor and other units, under low noise and low image lag applications.

2.5 Correlated Double Sampling (CDS)

As mentioned in above section, the correlated double sampling (CDS) is applicable for 4T APS, not in 3T APS, is used to achieve low noise performance. The CDS applied inside is

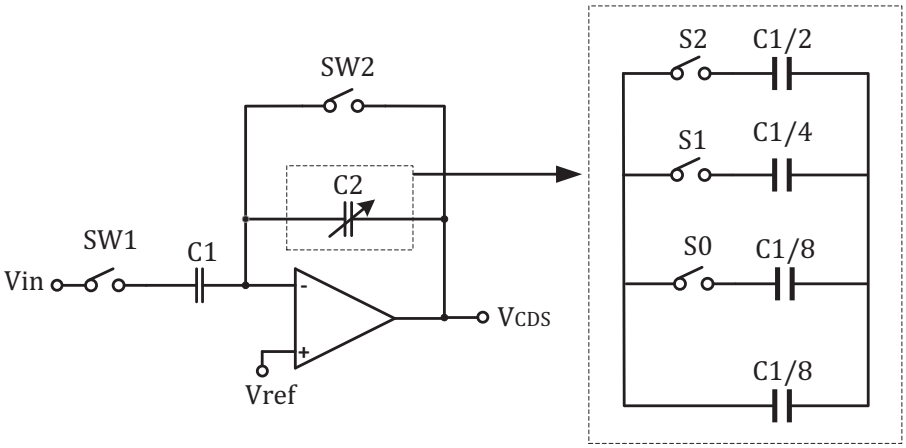


Figure 2.15: Correlated double sampling circuit.

used to eliminate thermal noise in the RC circuit generated in the reset transistor (M_{RST} of the PD, which is K_BTC noise. It also can suppress the fixed pattern noise (FPN) , as the FPN is mainly from the variation of the threshold voltage in in-pixel readout circuits. In order to cancel both noise ($V_N = V_{FPN} + V_{KTC}$), the CDS sample both reset charge ($V_{RST} + V_N$) and the signal charge ($V_{SIG} + V_N$) separately, and substract them to achieve the signal charge without effects caused at reset node/phase ($V_{SIN} - V_{RST}$). The circuit architecture of CDS is shown in Figure 2.15, which is consisted by an operational amplifier, two capacitors (C_1 and C_2) and several switches (SW1 and SW2).

The operation of CDS can be classified in two steps: (1) Sampling phase: the switch SW2 is turned on, the unity feedback of operational amplifier (op-amp) is formed. Meanwhile, the reset charge ($V_{RST} + V_N$) is sampled on capacitor C_1, and the charge in each capacitor are expressed as below:

$$\begin{aligned} Q_1 &= C_1 * (V_{ref} - (V_{RST} + V_N)) \\ Q_2 &= 0 \end{aligned} \qquad \text{(Eq. 2.15)}$$

(2) Amplification phase: the switch SW2 is turned off, as well as the unity feedback on op-amp. The new feedback of this op-amp is formed by capacitor C_2, and the charge

on C_1 will transfer to C_2. In this phase, the input for C_1 is signal charge from the pixel ($V_{SIG} + V_N$) and will be delivered into C_2 totally. As the minus input of this op-amp is tied to a voltage reference (V_{ref}, then the charge in each capacitor can be expressed as:

$$\begin{aligned} Q_1 &= C_1 * (V_{ref} - (V_{SIG} + V_N)) \\ Q_2 &= C_2 * (V_{out} - V_{ref}) \end{aligned} \qquad \text{(Eq. 2.16)}$$

The final output from CDS after two steps is calculated as follows:

$$V_{CDS} = V_{ref} + \frac{C_1}{C_2}(V_{RST} - V_{SIG}) \qquad \text{(Eq. 2.17)}$$

where the noise is cancelled by the subtraction ($V_{RST} - V_{SIG}$) through CDS circuits. The value V_{ref} added inside the CDS output normally is close to the common-mode voltage of the column-level analog circuitry. In real applications, since the highest value of subtraction ($V_{RST} - V_{SIG}$) should be V_{RST} when there is no light/charge accumulated in PD, and the lowest value should be close to zero when high density light/charge accumulated in PD. As well as the CDS output (V_{CDS}) cannot be lower than ground voltage and greater than the power supply. Thus, the ($V_{ref} + \frac{C_1}{C_2}V_{RST}$) should be lower than power supply and V_{ref} also cannot be very small which will disable the function of op-amp, then the value of V_{ref} can be set as value higher than the threshold voltage of transistor at input pair of op-amp, keeping the ($V_{ref} + \frac{C_1}{C_2}V_{RST}$) slightly lower than power supply.

Regarding the architecture of CDS as shown in Figure 2.15, the capacitor C_2 in CDS normally can be programmable to implement the CDS to amplify the signal, where the CDS is called as programmable gain amplification (PGA) [18]. Assuming the amplification gain is A, the input-referred noise will be suppressed as $\sqrt{V_{N2}/A}$, where V_{N2} is the noise in the signal chain after CDS circuit (mostly from ADC circuitry). As shown in Figure 2.15, the variable capacitance of C_2 can be implemented as:

$$
\begin{aligned}
C_2 &= \frac{C_1}{8} + \frac{S_0C_1}{8} + \frac{S_1C_1}{4} + \frac{S_1C_1}{2} \\
A = 1 &: C_2 = C_1(S_2S_1S_0 = \text{“}111''\text{)} \\
A = 2 &: C_2 = C_1/2(S_2S_1S_0 = \text{“}110''\text{)} \\
A = 4 &: C_2 = C_1/4(S_2S_1S_0 = \text{“}100''\text{)} \\
A = 8 &: C_2 = C_1/8(S_2S_1S_0 = \text{“}000''\text{)}
\end{aligned}
\qquad \text{(Eq. 2.18)}
$$

where the gain A is controlled globally. Normally, the value of gain is applied into entire pixel array, then the amplified signals are sent to ADC where the input referred noise before/after ADC are suppressed by this amplification.

Although the CDS cancels the FPN and thermal noise in pixel, but it also introduce another FPN noise caused by the offset voltage from the mismatch of differential pair in op-amp. Assume the offset voltage of op-amp is V_{offset}, the input voltage at minus sign of op-amp will be ($V_{ref} + V_{offset}$) which will added inside CDS output. Since the op-amp in the column-level CDS can not be exactly same, as well as the V_{offset}, so vertical stripe pattern will occur in the output image. In order to cancel this FPN, another CDS operation after this mentioned CDS, called 2^{nd} CDS, should be added inside the ADC. The ADC samples both $V_{ref} + V_{offset}$ (when CDS is in sampling phase) and $V_{ref} + V_{offset} + V_{SIG}$ (when in amplification phase), the subtraction of both values shows the clean voltage signal without the effects of V_{offset}. Thus, the desired V_{SIG} is obtained by 2^{nd} CDS.

2.6 Analog-to-Digital Converter (ADC)

In CMOS image sensor, the analog-to-digital converters (ADCs) have been integrated inside for the digital signal output. As shown in Figure 2.2 in first section, the column-parallel ADCs are implemented to quantize the analog pixel value into digital code.

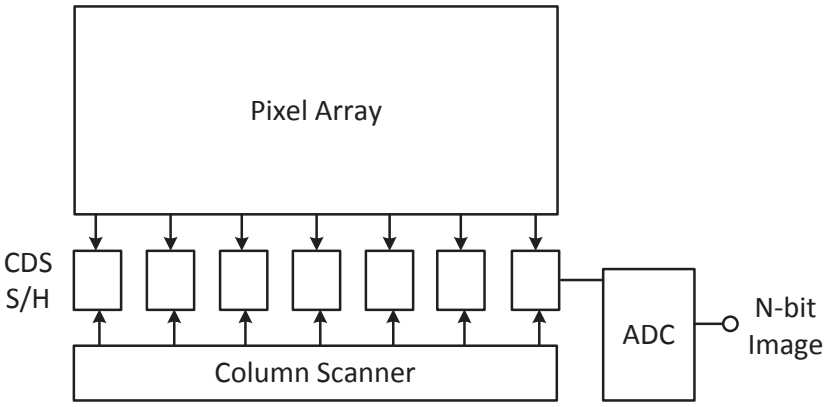


Figure 2.16: Implementation scheme of serial ADC in CMOS image sensor.

Actually, there are another two schemes to implement ADCs: serial ADCs and in-pixel ADCs, which are not widely integrated in CMOS image sensor nowadays. The architecture of those implementation schemes are illustrates in following section in detail.

2.6.1 Serial ADC

Serial ADCs, which is implemented beside of CMOS image sensor system as shown in Figure 2.16, converts the analog signals of entire pixel array serially. The pixel signals in pixel array are still processed row by row through the column-level CDS and sample-hold circuit (S/H), and later stored in the line buffer. Those analog signals in the line buffer are accessed serially by the column scanner, and be quantized into digital code through the serial ADC one by one. Thus, a high-speed ADCs are required, such as pipeline ADCs [6], as the speed bottleneck in the ADC will be a critical factor for high resolution of pixel array.

2.6.2 In-Pixel ADC

In-pixel ADCs convert the signal of all the pixel array at the same time, which is implemented inside the pixel [26]. As shown in Figure 2.17 The pixel signals in pixel array are quantized into digital code inside each pixel, later the digital code are processed row by

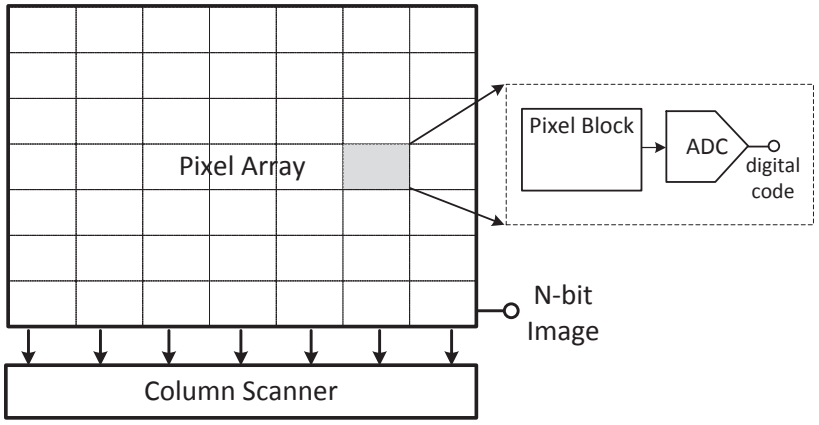


Figure 2.17: Implementation scheme of in-pixel ADC in CMOS image sensor.

row and stored into the lathes/memory in column level. Then those values stored inside latches/memory are readout and output as an image by the column scanner. Since all the analog signals of a pixel array are converted to digital code inside one A/D conversion period, which is much faster than the operation of serial ADC and column-parallel ADC. Thus, this scheme is more applicable for image sensor with high-speed requirement. As the ADC is implemented in pixel-level, it will consume large silicon area and it is not applicable for image sensor with large number of pixels.

2.6.3 Column-Parallel ADC

Column-parallel ADCs convert the signal of one row in parallel, which is implemented in the column-level and after the column-parallel CDS [3, 8, 16, 22]. The pixel signals in the pixel array are quantized into digital code row by row through CDS and ADC, then saved into the latches/memory in column level. Those digital value stored inside latches/memory are scanned out for reading by the column scanne and be used to form a frame. Since the pixels in one row are converted into digital code in one A/D conversion period, so the A/D conversion time for all the pixel signals in one array is dependent on the number of rows. The operating time of this scheme is much shorter than the serial ADC, but longer than in-pixel ADC.

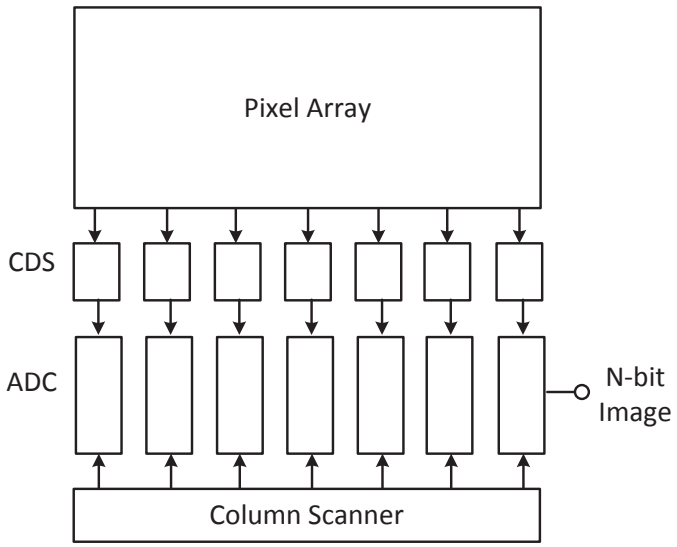


Figure 2.18: Implementation scheme of column-parallel ADC in CMOS image sensor.

Normally Cyclic ADCs,successive approximation (SAR) ADCs and single-slope (SS) ADCs are widely used for column-parallel ADCs [8, 16, 22]. Among them, SS ADCs are mostly widely used in CMOS image sensors, as they can be implemented with single comparator which is relatively easy to ensure the uniformity and implemented in fine pixel pitch as shown in Figure 2.19(a). The ramp generator is used to generate the global ramp reference for all the columns, the comparator in each column will compare the analog input with this ramp voltage until the comparison result trigger. And the counter at each column will store the time of trigger as shown in Figure 2.19(b) and later be converted into digital code based on the ADC resolution for readout and forming an image.

Based on the properties of those ADCs, the type of SAR ADC is chosen to be implemented in the proposed design, as its operating theory (binary searching tree algorithm), as well as its inherently low-power consumption. The background of SAR ADCs will be illustrated in detail in the next chapter.

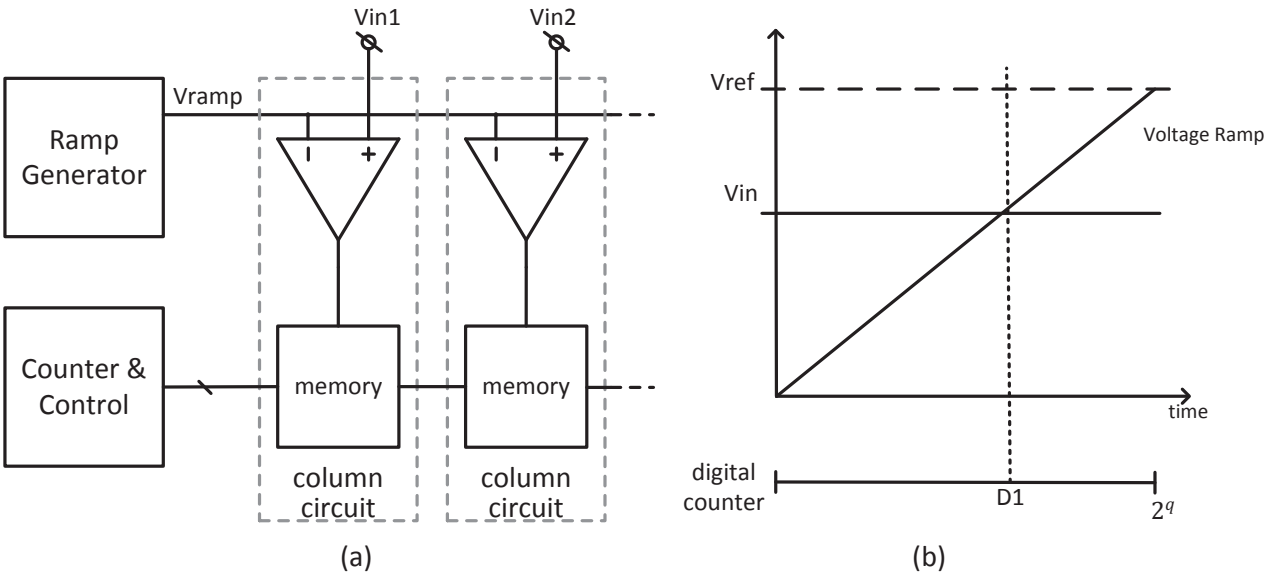


Figure 2.19: (Column-parallel single-slope ADC's (a) Architecture.(b)Timing diagram

Chapter 3

Introduction to Column-Parallel SAR ADCs

3.1 ADC Principle and Performance Metrics

Analog-to-digital converters (ADCs) are the interface between the analog input signal and digital signal processing block. The analog to digital conversion principles will be briefly reviewed in this section, the static and dynamic performance metrics of ADCs are presented [10, 13].

3.1.1 Resolution and Quantization Error

The resolution of ADC is defined by the number of bits at its output, where LSB is the least significant bit, MSB is the most significant bit. V_{LSB} is the smallest step, whose value is equal to $V_{REF}/2^N$ for an N-bit resolution ADC.

In an ADC, the quantization error is the difference between the analog input and converted analog value of ADC output via an ideal DAC. For an ideal ADC, the quantization step is 1 LSB which is $V_ref/2^N$, and the full-scale input range is -0.5V_{LSB} to (2^N-1)V_{LSB}. As shown in Figure 3.1, the digital output (D_{out}) is the sum of analog input (V_{in} and quantization error ($\varepsilon_q(V_{in})$. Regarding of a 3-bit ideal ADC input-output transfer curve based on full-scale analog input shown in Figure 3.1, the staircase curve is the

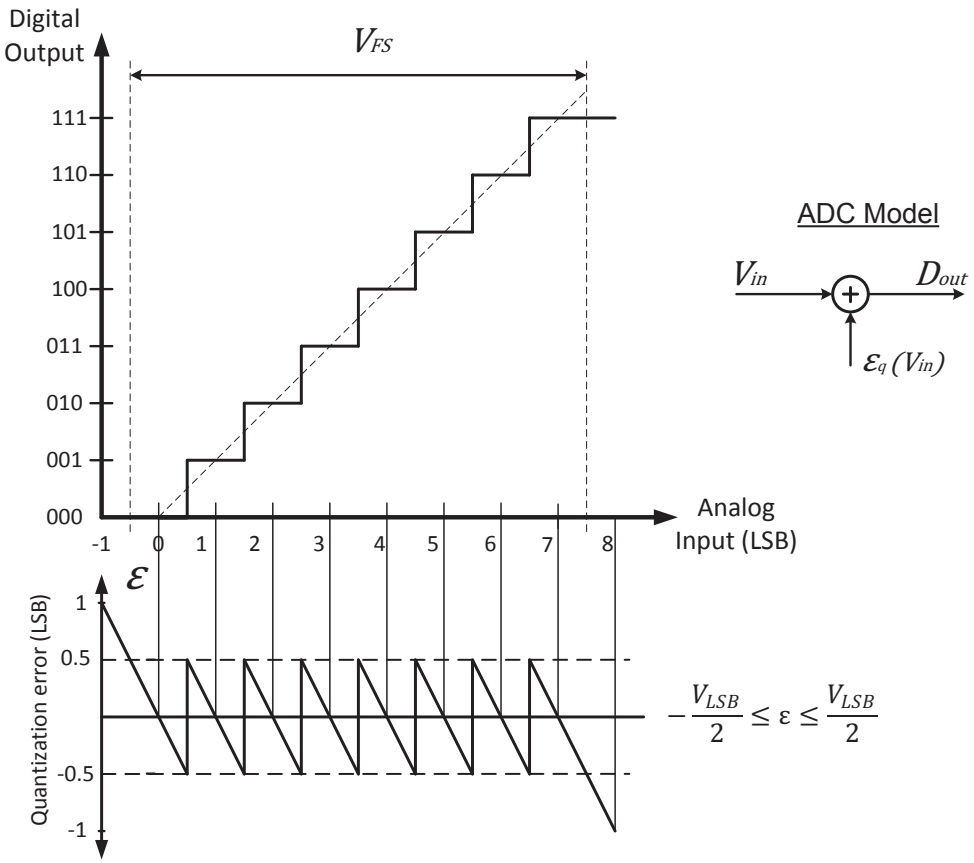


Figure 3.1: Quantization error of an ideal ADC.

digital output and the dashed line alined with it is the analog input. The quantization error is presented in the curve below, where the quantization error is in range vary from -V_{LSB}/2 to V_{LSB}/2 within the full-scale input range from -0.5V_{LSB} to 7.5$_{LSB}$. Thus, quantization error is also exist in an ideal ADC, and it can not be neglected.

3.1.2 Static Performance Parameters

Deviate from ideal, there are must be many defects introduced in real ADCs. So various parameters are used to determine the performance of an ADC, and they are broadly classified into two groups: static performance parameters and dynamic performance parameters. Those parameters that are not related to ADC's input signal are static parameters, and those related to input signal, frequencies are dynamic parameters.

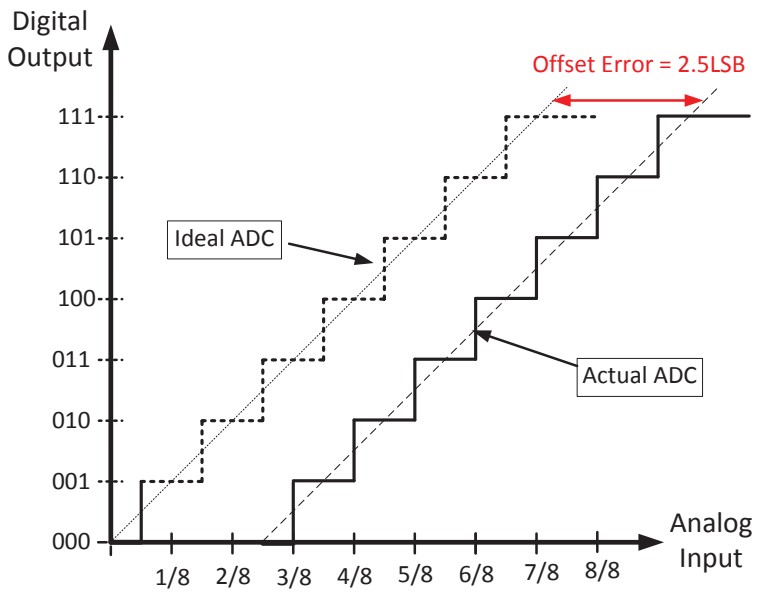


Figure 3.2: Offset error of a 3-bit ADC.

The major static parameters are formed by gain error, offset error, full-scale error and linearity errors.

3.1.2.1 Offset Error

The deviation of the actual ADC's transfer curve from the ideal ADC's transfer curve at the point of zero to one transition measured in LSB is defined as offset error. As shown in Figure 3.2, the transition from output value 0 to 1 does not occur at an input value of $0.5V_{LSB}$ for the actual ADC transfer curve, so there is an offset error for it and the difference between it and the ideal ADC transfer curve is defined as this error. Since the positive offset errors are detected when the output value is larger than 0 and less than $0.5V_{LSB}$, otherwise, the negative offset errors are detected. Therefore, the offset error for this case is negative error, which is $-2.5V_{LSB}$.

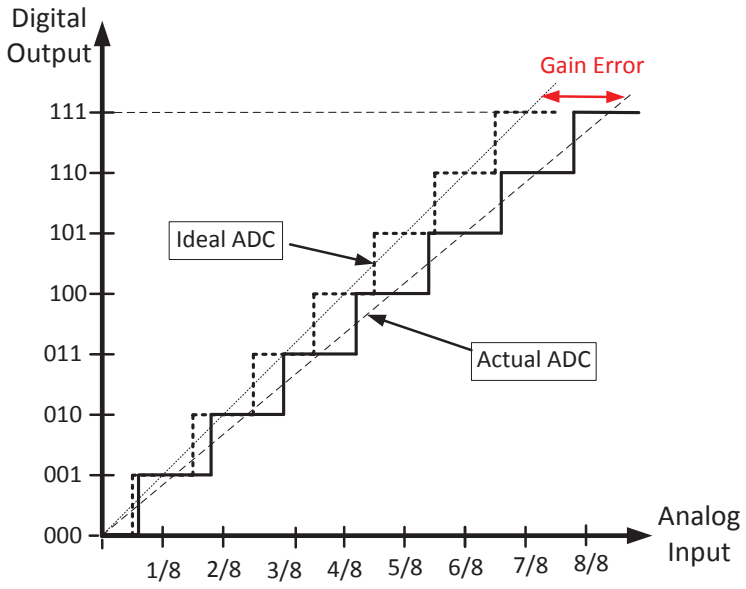


Figure 3.3: Gain error of a 3-bit ADC.

3.1.2.2 Gain Error

The error on the slope of the straight line interpolating the transfer curve is defined as gain error. As shown in Figure 3.3, the gain error is illustrated by using a 3-bit ADC input-output transfer curve. The slop for ideal converter is equal to D_{FS}/V_{FS}, where D_{FS} and V_{FS} are the digital code and analog input range in full scale (D_{111} and V_{in}) respectively. Thus, the deviation of the slopes between a actual ADC and a ideal ADC shown in Figure 3.3 is the gain error.

3.1.2.3 Full Scale Error

The full scale error is defined as the deviation of the last transition (full scale transition) between the actual ADC and the ideal ADC, which is results from both gain and offset errors. As shown in Figure 3.4, the full scale error is $1.5V_{LSB}$ based on the deviation of the last transitions of the actual ADC from the last transition of the ideal ADC.

Regarding the gain, offset and full scale errors mentioned above, they can be measure and compensated using some calibration methods in a ADC system.

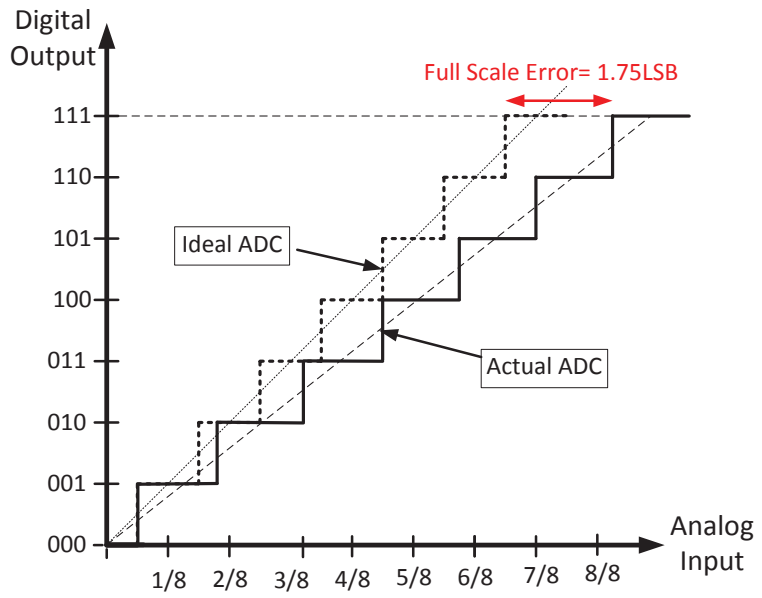


Figure 3.4: Full scale error of a 3-bit ADC.

3.1.2.4 Linearity Error

The gain and offset errors do not change the linearity of the transfer curve of a ADC, but the non-linearity may cause the actual curve to deviate slightly from the perfect curve which results the non linear transfer curve. Normally, the non-linearity is consisted by two major types: differential non-linearity (DNL) and integral non-linearity (INL).

The DNL is the deviation of the step size in a real ADC from the ideal width of an ideal ADC, where the ideal width is one LSB ($= V_{ref}/2^N$). As shown in Figure 3.5(a), the ideal ADC output is presented by dashed line and the actual ADC output is presented by solid line; the DNL for third step is one LSB where one code is missing, and for sixth step is -0.5LSB.

The INL is a measure of the deviation of the transfer curve from the ideal interpolating line, where the total INL is accumulated by the DNL errors, presented as below:

$$INL[k] = \sum_{i}^{k-1} DNL[i] \qquad \text{(Eq. 3.1)}$$

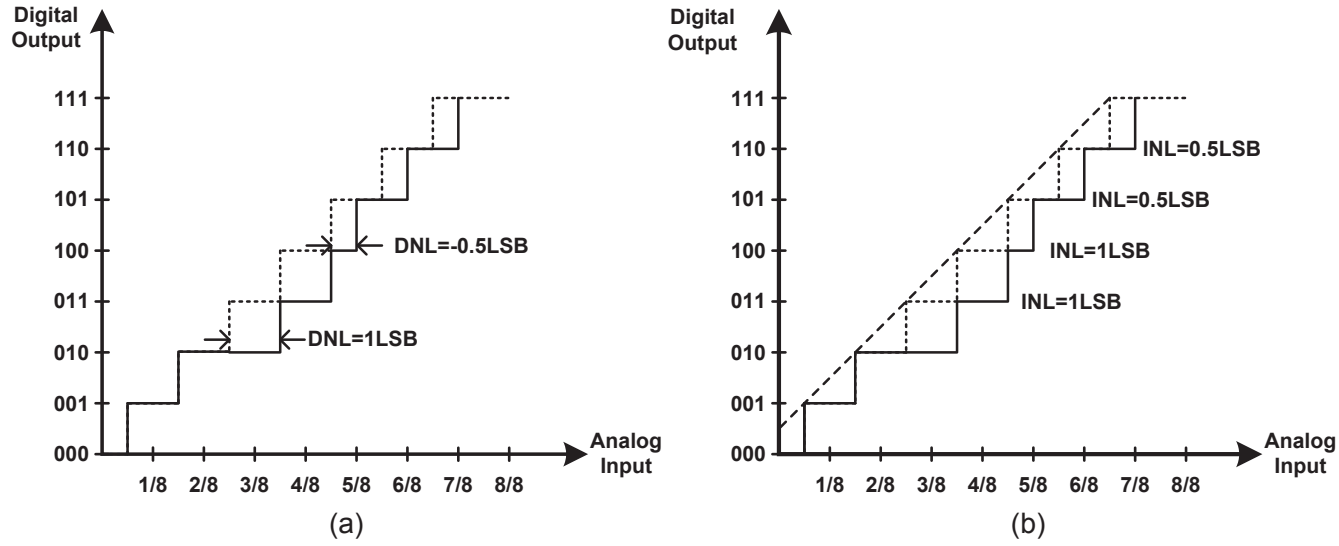


Figure 3.5: Non-linearity of a 3-bit ADC: (a) Differential (DNL), (b) Integral (INL).

where DNL[i] is the DNL for quantization step i, and INL[k] is the total INL for k quantization steps. The INL would be zero when the DNL for each step is not zero. As shown in Figure 3.5(b), the INL for fourth step is 1LSB and for seventh step is 0.5LSB. However, it is not possible to remove their effects with calibration, as DNL and INL are different based on each ADCs particular architecture.

3.1.3 Dynamic Performance Parameters

Regarding the dynamic parameters, it contains include signal-to-noise ratio(SNR), total harmonic distortion (THD), signal to noise and distortion (SINAD) and effective number of bits (ENOB).

3.1.3.1 Signal to Noise Ratio (SNR)

The ratio of the output signal voltage level to the output noise level is defined as signal to noise ration (SNR). It is calculated with the following formula and usually represented in decibels (dBs).

$$SNR(dB) = 20log(\frac{V_{RMS(Signal)}}{V_{RMS(Noise)}}) \quad \text{(Eq. 3.2)}$$

For example, if the output signal amplitude is 5V(root-mean-square (RMS)) and the output noise amplitude is 6mV(RMS), then the SNR value would be 58.42dB. The better performance of ADC, the higher the SNR value, and for an ideal ADC, the SNR should be given as:

$$SNR(dB) = 6.02 * N + 1.76(dB) \quad \text{(Eq. 3.3)}$$

where N is the resolution of the ADC. For an ideal 12-bit ADC, the SNR will be around 74dB.

3.1.3.2 Signal to Noise Ratio (Total Harmonic Distortion (THD))

The total harmonic distortion (THD) the term to define the effect caused by the additional contents added at the harmonics of the original frequency, whenever input sinal of a particular frequency passed through a non-linear device. For example, if the frequency is f for an input signal, and the harmonic frequencies are 2f, 3f, 3f, etc. Then the harmonics that were not present in the original sinal will be produced by the non-linearity in the converter, and those harmonic frequencies would also degrades the performance of the system as it usually distort the outputs.

In mathematical expression, the THD is defined as the ratio of the sum of powers of the harmonic frequency components to the power of the fundamental/original frequency component. The THD is given by the following formula in terms of RMS voltage:

$$THD = \frac{\sqrt{V_2^2 + V_3^3 + ... + V_n^2}}{V_1} \quad \text{(Eq. 3.4)}$$

Thus, the THD is affected by the input signal amplitude and frequency, as the distortion is higher with higher input signal amplitude. In order to have less distortion for the system, the THD should be minimized.

3.1.3.3 Signal to Noise Ratio (Singal to Noise and Distortion (SINAD))

The combination of SNR and THD parameters is defined as signal to noise and distortion (SINAD), which is the ratio of the RMS value of the signal amplitude to the RMS value of all other spectral components, including harmonics but excluding DC. So SINAD is a good choice to represent the overall dynamic performance of an ADC system, as it including both the noise and distortion compoenents.

Therefore, the SINAD can represented the formula below based on SNR and THD values:

$$SINAD = -10log(10^{-SNR/10} + 10^{-THD/10}) \quad \text{(Eq. 3.5)}$$

3.1.3.4 Signal to Noise Ratio (Effective Number of Bits (ENOB))

Effective number of bits (ENOB) is the number of bits of a actual ADC when it operated behaves like a ideal ADC. And its value is related to the noise and distortion of an ADC system, so it can be calculated based on the SINAD value:

$$ENOB = (SINAD - 1.76)/6.02 \quad \text{(Eq. 3.6)}$$

Regarding those dynamic parameters mentioned above, they are all used to quantify the distortion and noise of an ADC.

3.2 Column-Parallel SAR ADC

This section will illustrate the working principle and details of circuit blocks in column-parallel successive approximation (SAR) analog-to-digital converter (ADC) system. The simplified block diagram of a general SAR ADC is present in Figure 3.6, the analog input signal and voltage outputted from DAC are compared by a comparator, and the digital output of comparator would be fed back to successive approximation register after

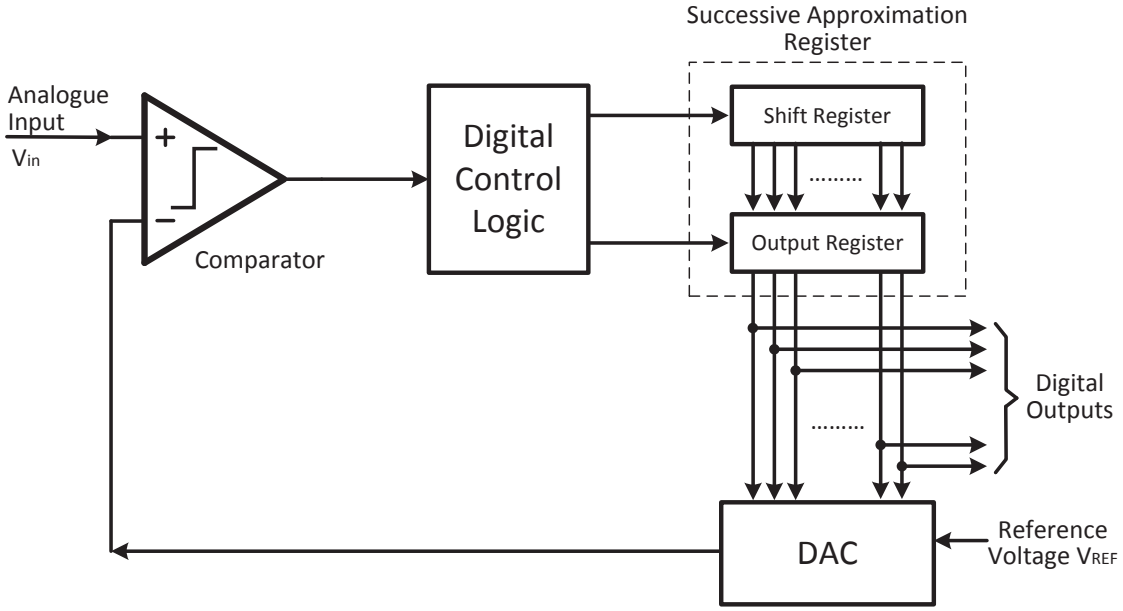


Figure 3.6: Block Diagram of SAR ADC.

a digital control logic to adjust the V_{DAC} with purpose to narrow down the difference between analog input and V_{DAC}. At the end of the conversion, the V_{DAC} is almost same as the analog input with the difference smaller than one V_{LSB}, the digital output from successive approximation register will be the quantization results for the analog input which will be read out.

3.2.1 Successive Approximation Algorithm

Successive approximation register ADC is operating based on binary search tree algorithm, which applied for converting analog input to a digital code. So each one digital bit is determined in one clock cycle through this successive approximation algorithm.

As shown in Figure 3.7(a), the first MSB would be determined first for a 3-bit SAR ADC, following with two results: 0 or 1. Then same working step is repeated until the last LSB is defined. The operation of this 3-bit SAR ADC with an analog input VIN is shown in Figure 3.7(b), in the first clock cycle DAC voltage is set to half of V_{ref} by setting the code to 100. Then the input voltage is compared to 1/2 V_{ref} and the first

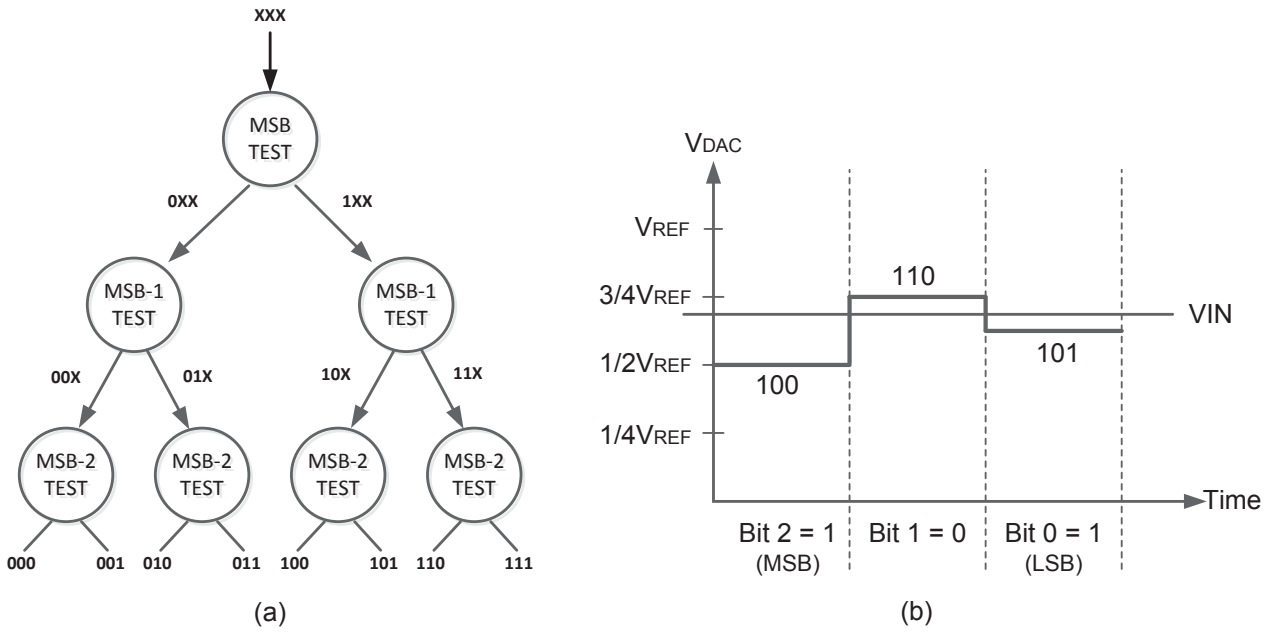


Figure 3.7: Successive approximation algorithm for a 3-bit SAR ADC.

MSB is defined based on the comparison result. If $V_{in} > V_{ref}$ /2, the fist MSB will not be changed and will remain at one, otherwise it would be reset to zero. So here MSB (D2) remains at one. The DAC voltage is set to 110 at next conversion cycle and V_{in} is compared to $3/4V_{ref}$, the D1 is set to zero as $V_{in} < 3/4V_{ref}$. For the last conversion, the V_{DAC} is set to 101, corresponding V_{DAC}=$5/8V_{ref}$, and D0 is set to 0 as comparison result. Therefore, the analog input is converted to the digital code 101 in three clock cycles.

3.2.2 Digital-to-Analog Converter (DAC)

Nowadays, a capacitive DAC are popularly be implemented in SAR ADCs as its inherent track/hold function. The capacitive DACs employ the principle of charge redistribution to generate an analog output voltage based on the digital code outputted from SAR control logic circuitry. The quantization results of a SAR ADC system is obtained by the comparison of this analog output voltage and input voltage through a comparator.

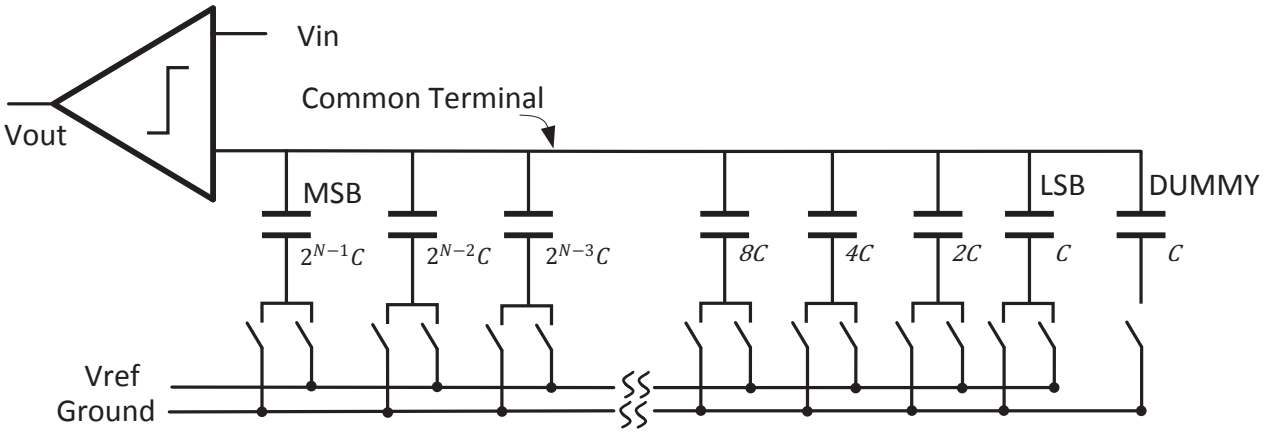


Figure 3.8: Equivalent Circuit of Capacitor Array.

Based on different specifications, there are several capacitor arrays applied in capacitive DAC are often used in the market, which are illustrated in the following section.

3.2.2.1 Binary-Weighted Capacitor Array

For binary-weighted capacitor array, this capacitive DAC consists of an array of N capacitors with binary weighted values plus one "dummy LSB" capacitor, as shown in Figure 3.8. It shows an N-bit capacitive DAC connected to a comparator, and this architecture has total 2^N unit capacitors where C is one unit capacitor.

Initially, both the top plate (common terminal shown in Figure 3.8) and bottom plate of capacitors are connected to ground for initializing all the capacitors. Later, the switches inside will switch to Vref in order from MSB to LSB which are controlled by successive shift register. The theory support this structure is the charge conservation, take MSB (C_N=2$^(N-1)$ C) for example, where the switch is connecting to Vref at N=1 and connecting to ground at N=0. The equivalent circuit of capacitor is shown in Figure 3.9 at case of N=1.

where $C_1 + C_2 = 2^N C$,

$C_1 = 2^{N-1}$, $C_2 = 2^{N-1}$.

Overall, the DAC output voltage can be evaluated as:

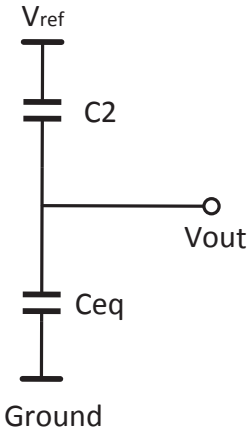


Figure 3.9: Equivalent Circuit of Binary Capacitor Array.

$$\begin{aligned} V_{out} &= V_{ref} * \frac{C_2}{C_1 + C_2} \\ &= \frac{2^{N-1}}{2^N} * V_{ref} \\ &= \frac{1}{2} * V_{ref} \end{aligned} \tag{Eq. 3.7}$$

As the binary-weighted capacitor array, for (N-1)=1, rest bits are zero:

$$\begin{aligned} V_{out} &= V_{ref} * \frac{C_2}{C_1 + C_2} \\ &= \frac{2^{N-1}}{2^N} * V_{ref} \\ &= \frac{1}{4} * V_{ref} \end{aligned} \tag{Eq. 3.8}$$

where $C_2 = 2^{N-2}C$, $C_1 + C_2 = 2^N C$. Therefore, the binary searching tree algorithm could be obtained based on the charging conservation theory.

3.2.2.2 Split Binary-Weighted Capacitor Array

The capacitive DAC with split-capacitor architecture, it consists two binary-weighted arrays connected via a series unit capacitor. In terms of an N-bit DAC, it contains one

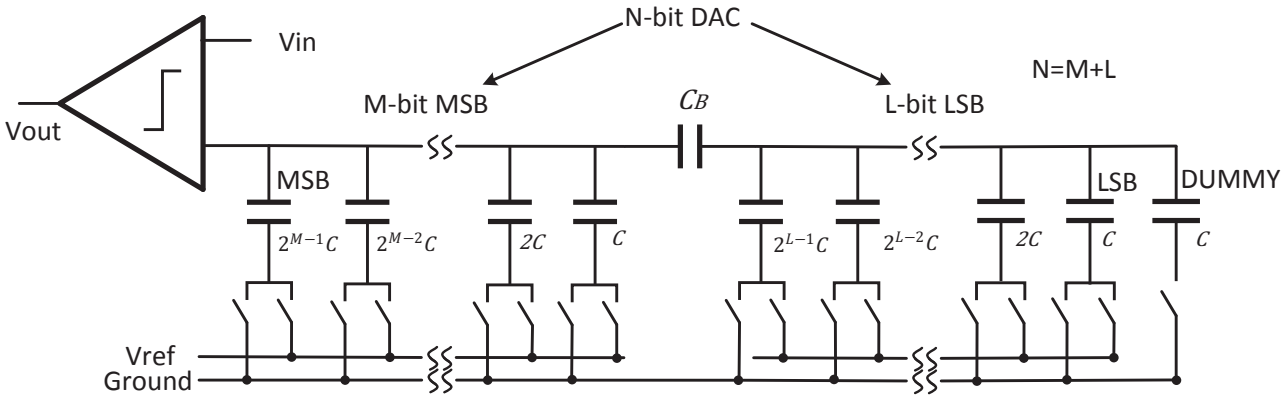


Figure 3.10: A N-bit split-capacitor capacitive DAC.

L-bit LSB and one M-bit MSB arrays (where M+L =N), which have 2^L and (2^M-1) unit capacitors respectively.

Initially, both the top plate (common terminals at both MSB and LSB sections as shown in Figure 3.11) and bottom plate of capacitors are connected to ground for initializing all the capacitors. Later, the switches inside will switch to V_{ref} in order from MSB to LSB which are controlled by successive shift register. The total capacitance of C_B and L-bit LSB section should be equivalent to a unit capacitor, in order to keep the C_total=2^M*C for the conversion steps in M-bit MSB section. Therefore:

$$\begin{aligned} C_B//(2^L)C &= C \\ C_B &= \frac{2^L}{2^L-1} * C \end{aligned} \qquad \text{(Eq. 3.9)}$$

Based on the charge conservation, take MSB ($C_N = 2^{M-1}$ C) for example, the equivalent circuit of capacitor is shown in Figure 3.9 at case of N=1.

Where $C_1 + C_2 = 2^N C$,

$C_1 = 2^{M-1}C$, $C_2 = 2^{M-1}C$.

Overall, the DAC output voltage can be evaluated as:

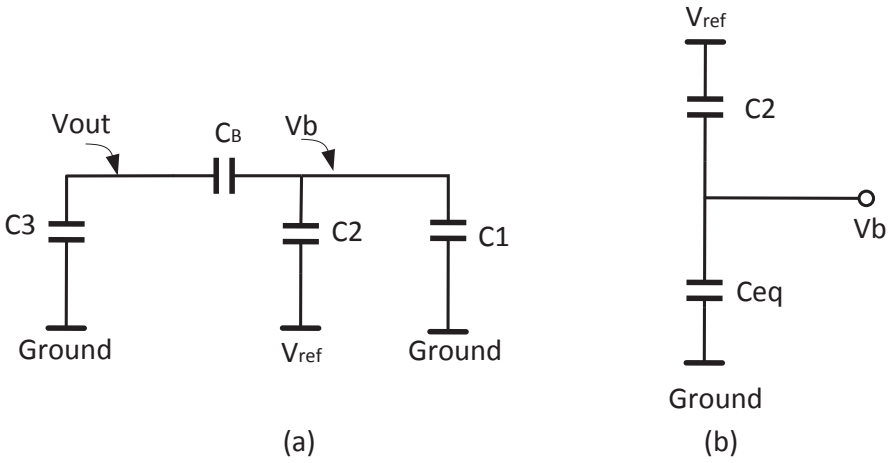


Figure 3.11: Equivalent Circuit of Split Capacitor Array.

$$\begin{aligned} V_{out} &= V_{ref} * \frac{C_2}{C_1 + C_2} \\ &= \frac{2^{N-1}}{2^N} * V_{ref} \\ &= \frac{1}{2} * V_{ref} \end{aligned} \qquad \text{(Eq. 3.10)}$$

Based on the same method, the conversion step of MSB section could be evaluated. Regarding the conversion steps on LSB section, for bit L (first MSB in LSB section), the equivalent circuit of capacitor is shown in Figure 3.11 at case of L=1.

Where $C_3 = (2^M - 1) * C$,

$C_2 = 2^{L-1}C$, $C_1 = 2^{L-1}C$.

As shown in Figure 3.11(b), $V_{eq} = C_1 + C_3//C_B$, where $C_B = (2^L/2^{L-1}) * C$.

$$\begin{aligned} V_b &= \frac{C_2}{C_2 + C_{eq}} * V_{ref} \\ V_{out} &= \frac{C_B}{C_B + C_3} * V_b \\ V_{out} &= \frac{2^{L-1}}{2^N} * V_{ref} \end{aligned} \qquad \text{(Eq. 3.11)}$$

The rest LSB bits will be evaluated based on it, and they are also satisfied the binary searching theory. Comparing to the binary-weighted capacitive DAC, it reduces the total capacitance and the DAC switching power significantly, because the switching power is contributed more with higher capacitance.

$$\begin{aligned} C_{total} &= (2^M + 2^L - 1) * C + C_B \\ &= (2^M + 2^L + \frac{1}{2^L - 1}) * C \\ &<< 2^N * C \end{aligned} \qquad \text{(Eq. 3.12)}$$

The M and L normally have same number value in the general design to achieve the smallest number of total unit capacitors. For binary-weighted architecture, the parasitic capacitance is not a problem, but it poses severe performance limitation to the split-capacitor architecture due to the capacitor C_B. Any parasitics caused by C_B, the top plate will change the capacitor ratio or the radix of LSB part with C_B, which will creates a limitation in the achievable resolution if not solved properly. Normally, the calibration schemes either in analog or digital domain has proposed to solve this problem, or increase the unit capacitance in a reasonable region to parasitic effects.

3.2.2.3 C-2C Capacitor Array

The C-2C capacitive DAC is similar to the widely known R-2R DAC and the schematic of a N-bit charge redistribution SAR ADC with C-2C is shown in Figure 3.12 [24]. There are only two capacitance sizes of C and 2C are used inside, the capacitor C on the leftmost of the array is the "dummy LSB" its neighbor capacitor C is the LSB, and the rightmost capacitor C is the MSB. The total capacitance for an N-bit capacitive DAC is calculated as:

Based on the charge conservation, take MSB (C_N=C) for example, the equivalent circuit of capacitor is shown in Figure 3.9 at case of N=1.

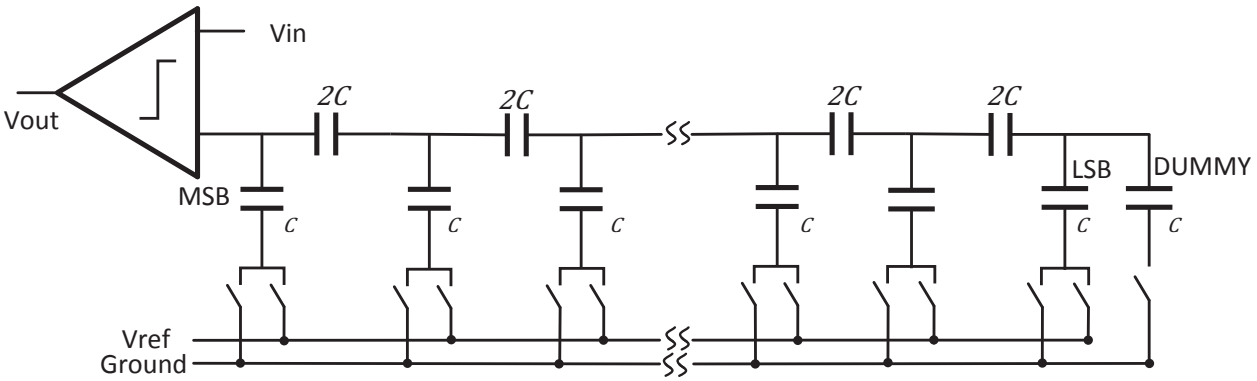


Figure 3.12: A N-bit DAC with C-2C capacitor.

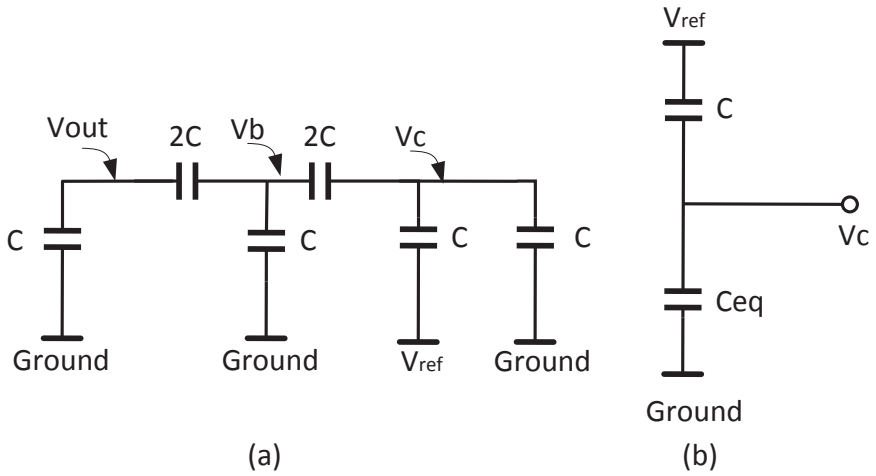


Figure 3.13: Equivalent Circuit of C-2C Capacitor Array.

Where $C_1 + C_2 = 2C$,

$C_1 = C$, $C_2 = C$.

Overall, the DAC output voltage can be evaluated as:

$$V_{out} = \frac{C_2}{C_1 + C_2} * V_{ref} = \frac{1}{2} * V_{ref} \qquad \text{(Eq. 3.13)}$$

Regarding the conversion steps on (N-2) bit, the equivalent circuit of capacitor is shown in Figure 3.13 at case of (N-2) =1. As shown in Figure 3.13(b), $C_{eq} = (C + 2C//C)//2C + c = 21/11 * C$.

$$\begin{aligned} V_b &= \frac{C}{C + C_{eq}} * V_{ref} \\ &= \frac{2C}{2C + C + 2C//C} * V_c \\ &= 6/11 * V_c \end{aligned} \quad \text{(Eq. 3.14)}$$

Therefore:

$$\begin{aligned} V_{out} &= \frac{2C}{3C} * V_b \\ &= 2/3 * 6/11 * V_c \\ &= 1/8 * V_{ref} \end{aligned} \quad \text{(Eq. 3.15)}$$

Based on the calculation, the rest of the bits will also be evaluated and satisfied the binary searching algorithm. Comparing to previous two architectures, the C-2C ladder-based DAC architecture is very attractive because of its small total capacitance which resulting small silicon area and low power consumption.

$$\begin{aligned} V_{total} &= (N+1) * C + (N-1) * 2C \\ &= (3N-1) * C \\ &<< 2^N * C \end{aligned} \quad \text{(Eq. 3.16)}$$

Same as split-capacitor architecture, the parasitic capacitance caused by those 2C limit the performance of C-2C DAC. Because the parasitics caused by each 2C will change the capacitor ratio between 2C and its right side capacitors, so the radix of top plate in the DAC will be modified and it is different for each bit. This creates a big limitation in the achievable resolution if without any calibration schemes applied, and its calibration is also more complex than split-capacitor one. Thus, C-2C SAR ADCs are still limited to low-medium resolution and not as popular as previous two architectures.

3.2.3 SAR Logic Operation

The binary search algorithm is implemented in successive approximation register ADC through SAR control logic. In general, there are mainly two fundamentally different approaches to designing the SAR logic circuitry. One is proposed by Anderson, which is consisted of a ring counter and a shift register, with at least 2N flop flops for an N-bit successive approximation register [1]. The other one proposed by Rossi, which contains N flip flops and other combinational logic [20].

SAR control logic operation could be represented by a sequential Finite State Machine, as it is used to determine the values of bits for ADC sequentially based on the results of the comparator. It is illustrated in Table 3.1, where the column shows the number of clock cycles, the second column presents whether the operation is under sampling phase or not, the third column illustrates values assigned to DAC from SA register, and the last column shows the comparison result between the DAC output and analog input.

Table 3.1: Finite State Machine Algorithm

Cycles	**Sample**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Comp**
0	1	0	0	0	0	0	0	0	0	0	0	-
1	0	1	0	0	0	0	0	0	0	0	0	a_9
2	0	a_9	1	0	0	0	0	0	0	0	0	a_8
3	0	a_9	a_8	1	0	0	0	0	0	0	0	a_7
4	0	a_9	a_8	a_7	1	0	0	0	0	0	0	a_6
5	0	a_9	a_8	a_7	a_6	1	0	0	0	0	0	a_5
6	0	a_9	a_8	a_7	a_6	a_5	1	0	0	0	0	a_4
7	0	a_9	a_8	a_7	a_6	a_5	a_4	1	0	0	0	a_3
8	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	1	0	0	a_2
9	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	1	0	a_1
10	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	1	a_0
11	0	a_9	a_8	a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0	-

At cycle 0, it is the sampling phase of analog input, where the values of 10-bit digital output are initialized to zero and no comparison output. At cycle 1, D9 is set to 1 first, and the corresponding DAC output compares to analog input resulting comparison result

a_9. Later the a_9 is written into D9, meanwhile D8 is set 1 and the comparison result is updated to a_8. Following the same operating methodology, the 10-bit comparison results are written in to D9 to D0 accordingly within 11 clock cycles. Therefore, 12 clock cycles are required for a 10-bit SAR A/D conversion cycle.

3.2.3.1 SAR Logic Type 1

The SAR control logic presented in [1] is shown in Figure 3.14, which is commonly used in SAR ADCs due to its straightforward design technique. This design consists of a ring counter and a code register, where the ring counter is in fact a shift register. For an SAR ADC conversion, at the clock cycle 0, the Reset signal is high and all the Flip Flops are reset and output values are zero, for the rest of cycles shown in Table 3.1, the Reset signal is low. At the rising edge of the clock, the Flip Flop (down side in Figure 3.14) loads the result from comparator inside. Besides, at the last clock cycle, all the outputs of Flip Flops (down side) would be written to elsewhere, like memory. Finally, the reset signal will be turned to high again for next ADC conversion. There has 12 clock cycles needed to converts each sample in this type of SAR logic. The advantage of this architecture is its low power due to low signal transition, it also can be extended to higher resolutions by just extending the shift registers since this logic is iterative.

3.2.3.2 SAR Logic Type 2

The SAR control logic mentioned in [15] as shown in Figure 3.15, needs at least N Flip Flops (FFs) to perform conversion for an N bit SAR ADC. So the non-redundant SAR employs minimum number of flip flop. In this design, the FFs both guess and store the converted results, at the initialization step (step 0), the first MSB is assigned to 1 and rest to be 0, which is equivalent to $V_{ref}/2$ after D/A converter. At the rest steps, the SAR control logic makes decision based on the output of the comparator. If it is

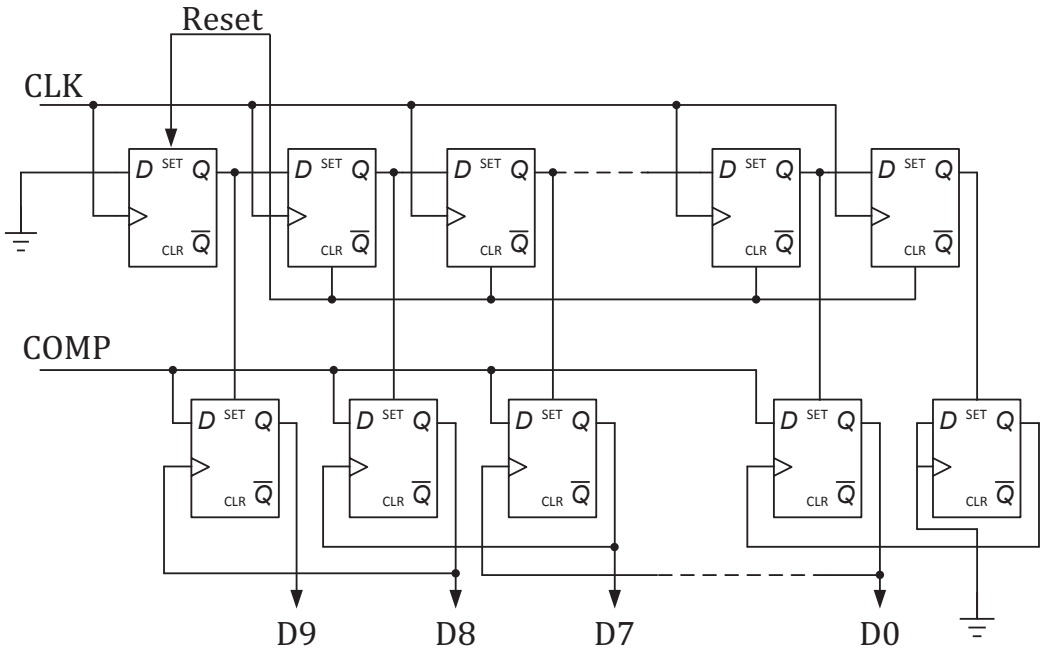


Figure 3.14: Successive approximation logic [1].

high, the select bit remains one, otherwise changes to zero. All the digital bit values are determined by the SAR logic sequentially.

As shown in Figure 3.15, this design contains an N-bit shift register and OR chain, and there are three possibilities for each bit, (i) Shifting right, (ii) taking the comparator results and (iii) memorization mode. Thus, each flip flop could take the result of the comparator, the output of the previous flip flop, or the value of the OR gate in each step. In terms of its operation, the first flip flop on the left should be set to one and the rest to zero at initialization state, which can be set by an external control signal called start signal. In the following steps, since there are three possible inputs for each flip flop, where only one possibility is taken, so a three input 3:1 MUX is required. The appropriate inputs is selected according to the Table 3.2. Furthermore, the conversion is terminated by applying high voltage to the OR chain, where SAR enters the storing mode. It is performed by connecting the output of the last flip flop to the OR chain, which means the end of conversion is defined by the least significant flip flop on the right.

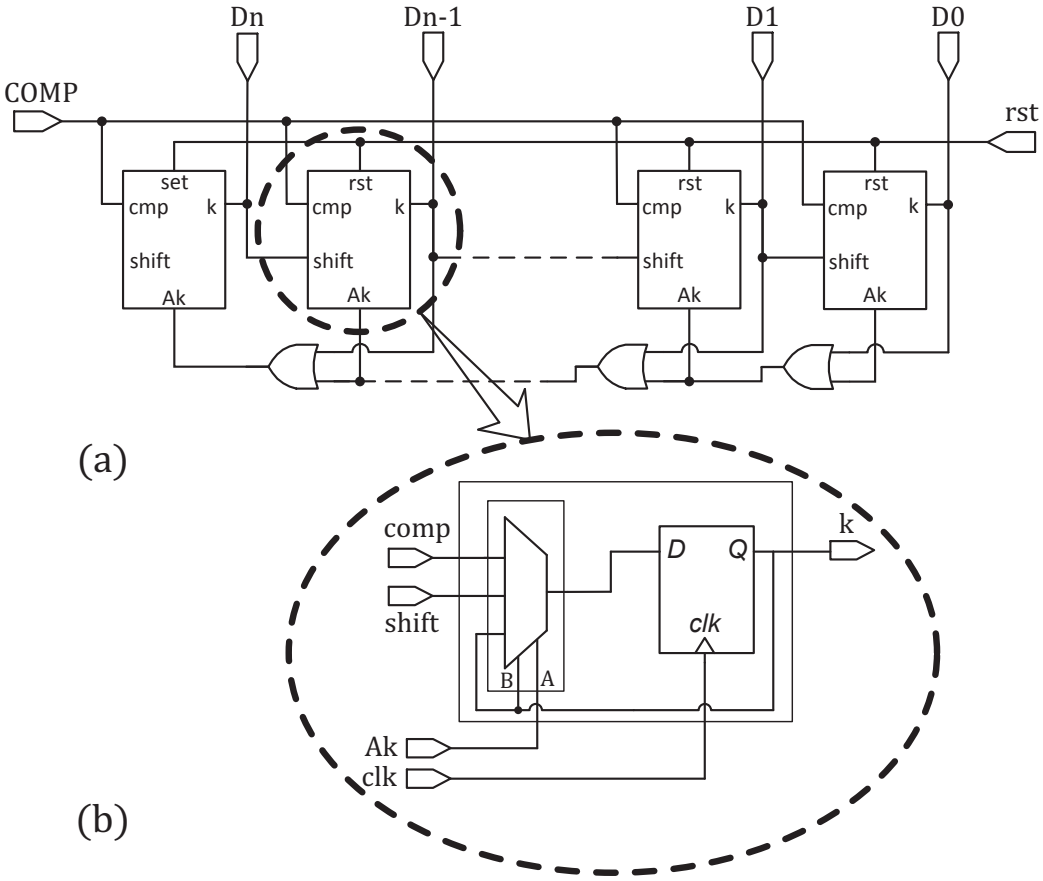


Figure 3.15: Successive approximation logic [20].

Table 3.2: Selection Mode of 3:1 MUX

A	B	
1	-	Memorization
0	1	Data Load
0	0	Shift Right

This architecture is also iterative, the higher resolution can be obtained by extending the sequences of FFs. But the starting signal required specially in this design should be adjusted manually for different clock frequencies, which can be mitigated by adding a counter to this structure.

Chapter 4

Design of Low-Power Column-Parallel ADC system for CMOS Image Sensors by Leveraging Spatial Likelihood in Natural Scene

Based on the spatial likelihood feature of most natural scenes introduced in Chapter 1, the design of a low-power column-parallel ADC system using a prediction scheme is described in this chapter. Both the low power algorithm and hardware implementation will be discussed in detail. Firstly, the algorithm and operation principle of the proposed prediction scheme are discussed. This is followed by the discussion of system architecture for hardware implementation. Lastly, the column-parallel SAR ADC system using the prediction scheme is described in detail, including block diagrams of a SAR ADC, architecture of DAC, timing diagram of successive approximation (SA) register, and architecture of comparator.

4.1 Proposed Algorithm of the Prediction Scheme

In the novel SAR DAC architecture, we proposed a prediction scheme by taking advantage of this likelihood correlation in most natural scenes and sequential readout manner in CMOS image sensors to reduce switching energy of SAR ADCs. The proposed prediction

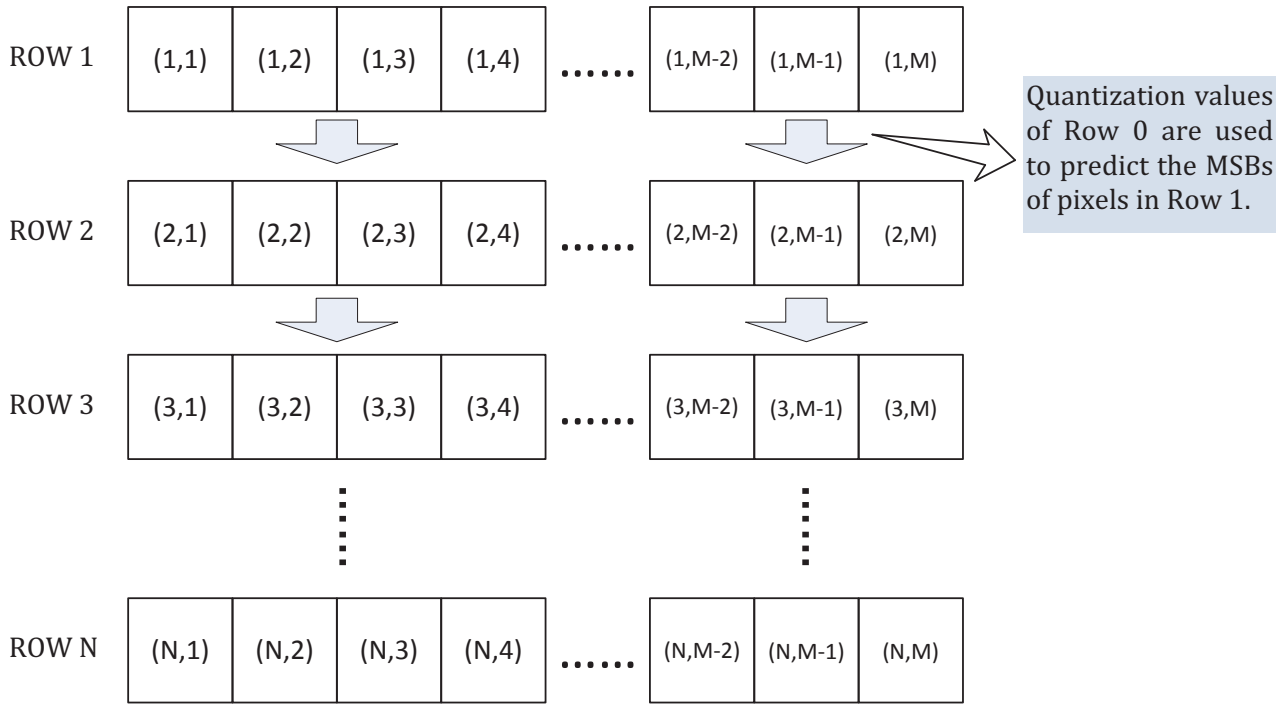
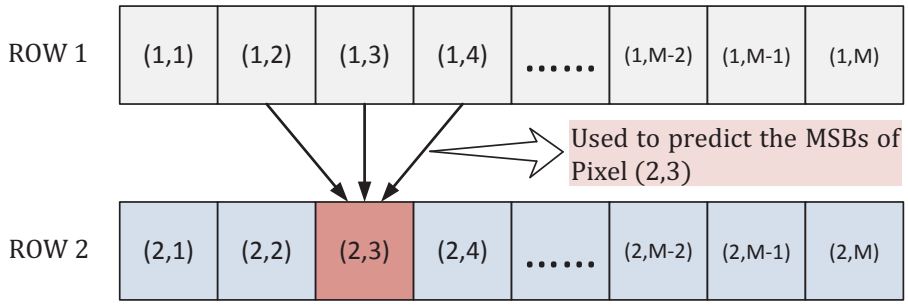


Figure 4.1: The illustrative explanation of the proposed prediction scheme using a N × M pixel array.

scheme primarily predicts the pixels ADC values row-wisely, more precisely their MBSs, based on the quantization values in the previous row.

Figure 4.1 illustrates the algorithm of proposed prediction scheme implemented in an image sensor with pixel array (N rows × M columns). Initially, pixels in first row are quantized by a conventional A/D conversion cycle as no historical quantization results are used to predict MSBs for them. When it comes to second row, the MSBs of pixels are predicted by quantization values of first row, and left LSBs are quantized by A/D conversion steps. Likewise for the third row, and a digital frame is generated after obtaining the quantization values of pixels in the last row.

Figure 4.2 illustrates the operating details of a prediction scheme, where the MSBs of a certain pixel are predicted using quantization values of its three neighbor pixels in previous row. Using Pixel (2,3) in second row as an example, the MSBs of it are



Pixel (1,2)	1	0	1	0	1	1	0	0	0
Pixel (1,3)	1	0	1	0	0	1	0	1	0
Pixel (1,4)	1	0	1	0	1	0	1	1	1
Common MSBs (m bits)	1	0	1	0	X	X	X	X	X
Predicted MSBs (m-1 bits)	1	0	1	X	X	X	X	X	X

Figure 4.2: The procedure to generate the predicted MSBs for a selected pixel with a 9-bit ADC.

estimated using quantization values of Pixel (1,2), (1,3) and (1,4) in first row, where they are the neighbor pixels of Pixel (2,3) in previous row. Due to the assumption of spatial likelihood, these pixels are likely to have the same MSBs. In this example the common MSBs for pixel (1,2), (1,3) and (1,4) is 1010, where the values of Pixel (1,2), (1,3) and (1,4) are 101011000, 101001010 and 101010111 respectively shown in the table of Figure 4.2. The next step is to estimate the MSB of Pixel (2,3) from the common MSBs. It is straightforward to directly use the common MSBs as MSBs of Pixel (2,3). The proposed method however utilizes one bit less of the common MSBs as predicted MSBs to increase success rate of the prediction scheme. The predicted MSBs of Pixel (2,3) is 101XXXXXX in this example.

Based on the operation principle of ADCs, two reference voltages (forming a voltage window) are utilized as voltage range of an analog input which is able to be quantized by the ADC. Implementing the prediction scheme in an ADC system, the predicted MSBs

are converted to analog value which is the starting reference voltage. Using Pixel (2,3) as an example, the starting reference voltage is $5/8V_{ref}$ converted from the predicted MSBs (101XXXXXX = 101000000). As the predicted MSBs are frame dependent and different for different pixels. The starting reference voltages of following A/D conversion predetermined by them are also frame dependent. It is complex to generate them before A/D conversion. Architecture of Column-parallel SAR ADCs is the most suitable architecture to implement the prediction scheme, because of SAR ADCs track/hold function of the capacitive DAC. The DAC in a SAR ADC generates the starting reference voltages before A/D conversion by assigning predicted MSBs into the capacitors of DAC. The operation principle of a SAR ADC is based on the binary search tree algorithm, so the starting searching bit of an A/D conversion cycle is not only first MSB, but also any bit between first and last bit. The operating procedure of SAR ADC with the prediction scheme is shown in Figure 4.3(a), and the successive approximation searching steps for Pixel (2,3) shown in Figure 4.2 are illustrated in Figure 4.3(b).

As shown in Figure 4.3(a), the common MSBs of three neighbor pixels in the previous row for a selected pixel are generated first, then one bit less of this common MSBs (m-1 bits) are assigned into the capacitive DAC of a SAR ADC to generate the starting voltage level for upcoming A/D conversion. After achieving final quantization results through A/D conversion, the correctness of the prediction is evaluated. For example, two analog inputs (V_{in1} and V_{in2}) shown in Figure 4.3(b), with same predicted MSBs (101XXXXXX). One of analog inputs (V_{in1})is predicted correct and one (V_{in2}) is predicted incorrect.

Figure 4.4 illustrates the A/D conversion steps of a 5-bit SAR ADC, where Figure 4.4(a) shows five A/D conversion steps of the ADC and Figure 4.4(b) shows seven A/D conversion steps of the ADC with two more LSBs. If final quantization value is converge to the analog input, the oscillation appears at last three moving steps shown in

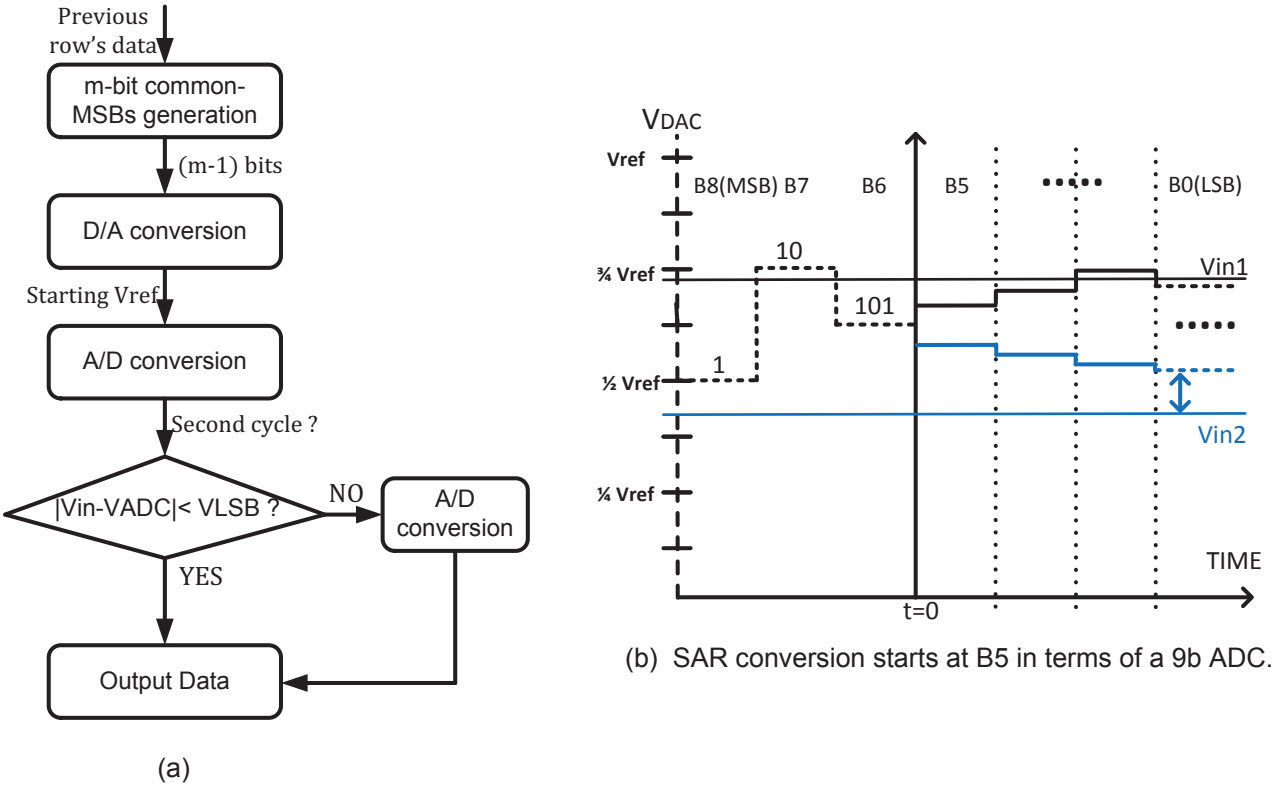


Figure 4.3: (a) Operation principle of a SAR ADC system with prediction scheme. (b) SA searching steps of an example with a 9-bit ADC.

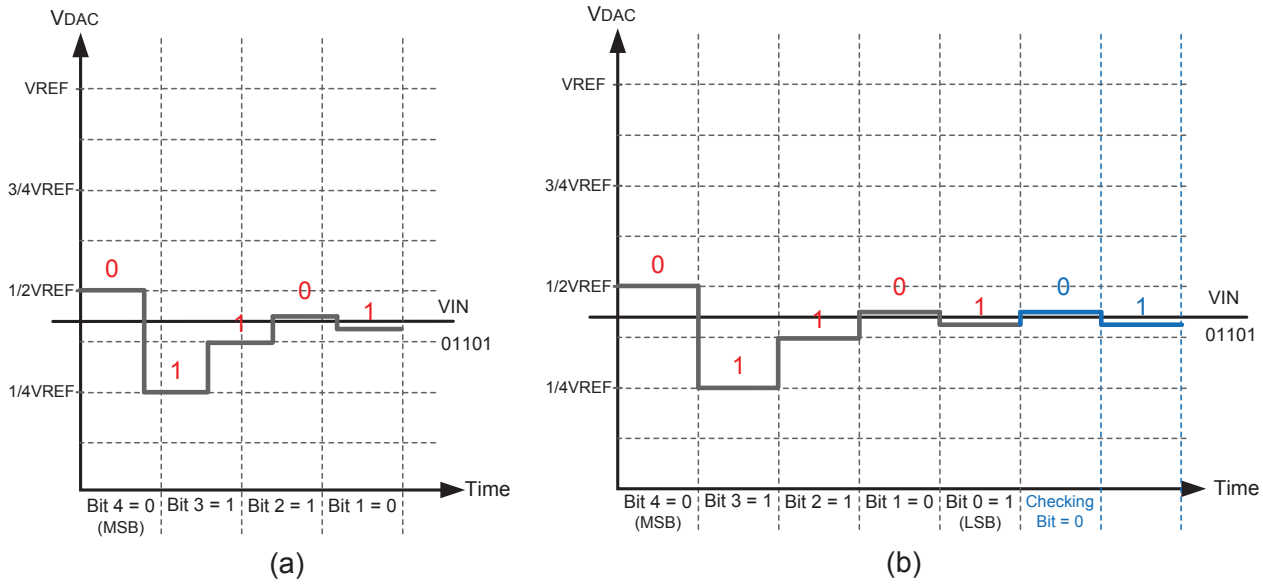


Figure 4.4: (a) A/D conversion steps of 5-bit SAR ADC. (b) A/D conversion steps of 5-bit SAR ADC with two more LSBs.

Figure 4.4(b), and last three moving steps size are same. Thus, the oscillation is used to determine the correctness of final quantization value, and the predicted MSBs. Only one extra LSB conversion step is added after conventional A/D conversion steps in real design, which is called as checking bit as shown in Figure 4.4(b). The predicted MSBs are correct if this checking bit quantization value is not same as LSB value. In other word, the difference between analog input and analog value of final quantization is less than one V_{LSB} (where V_{LSB}=$V_{ref}/2^N$), if the final quantization value is converge to analog input. So if this prediction is correct (like V_{in1} shown in Figure 4.3(b)), the values of last LSB and checking bit are different. The final quantization value with prediction is saved into memory temporarily, for being read out and used to generate the predicted MBSs for pixels next row. Otherwise (like V_{in2}), the values of last LSB and checking bit are same and the final quantization value with prediction is discarded. A new A/D conversion cycle starting from first MSB is used to obtain the new quantization value, which are stored into memory.

4.2 Sensor Architecture and Implementation

A CMOS image sensor system with column-parallel ADCs using the prediction scheme is proposed, and the architecture of this sensor is described in this section. As shown in Figure 4.5, this architecture consists of a pixel array, column-parallel correlated double samplings (CDSs), a 9-bit column-parallel SAR ADC system and two sets of memory banks, a row scanner, and digital controller circuitries. In this design, one memory bank (MEM 1) is used to store the quantization results, which are scanned out for reading. The one (MEM 2) is used to store the quantization values of pixels in previous row for MSBs prediction.

4.2.1 Pixel and Column Circuitry

As shown in Figure 4.5, the 4-T APS architecture is used in this design, because of its high sensitivity obtained by the amplifying action of the TX transistor. It also enables CDSs to cancel the reset noise (as mentioned in Chapter 2). The CDSs are added in every column to cancel the reset noise for this design.

The layout of a 4-T APS implemented inside the CMOS image sensor is presented in Figure 4.6, the green layer indicates diffusion, the blue, white and yellow layers represent Metal 1, 2, 3 respectively, red layer signifies poly 1, and those small square blocks indicate vias which are used to connect neighboring layers. The photodiode is the most important component in a 4-T APS, whose size in layout should be maximized and kept as rectangular. It is highlighted in red rectangular in Figure 4.6, which is used to capture the light information and calculate the fill factor of a pixel. The physical implementation of this photodiode was n+/Nwell/P-sub, the diode was formed by Nwell/p-sub, the extra n+ layer was used to transfer the charge accumulated in diode to transistors. The four transistors used in 4-T APS were designed as small as possible, as long as the left silicon area beside the photodiode is able to contain three horizontal wires representing

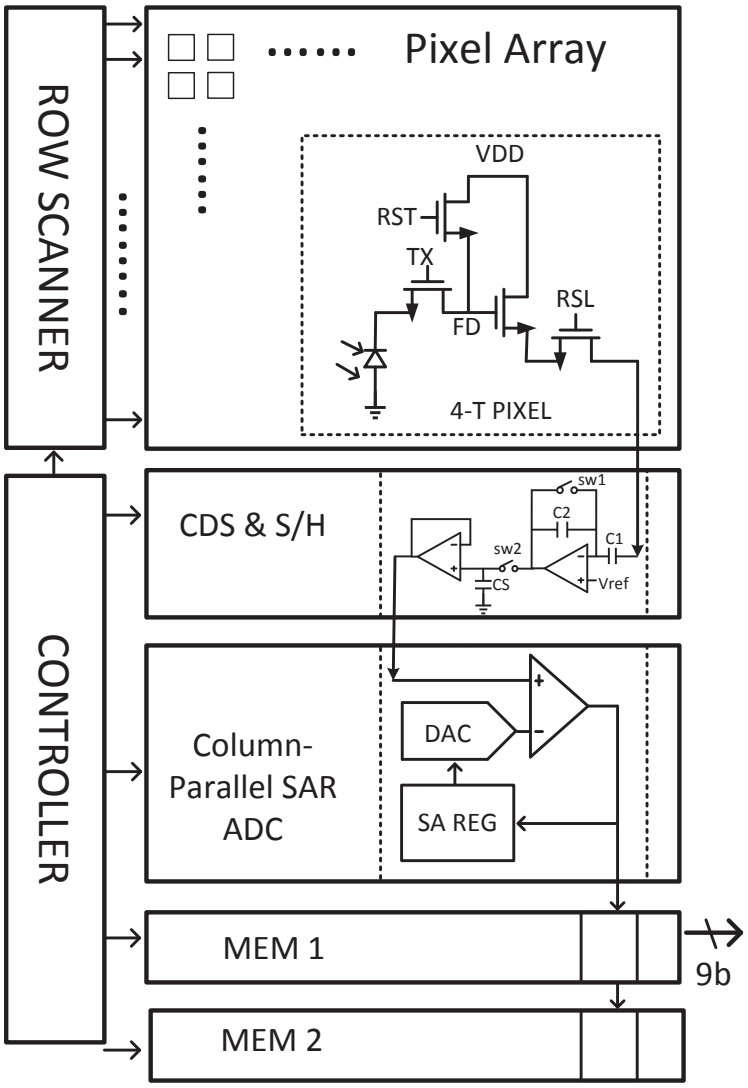


Figure 4.5: Block diagram of CMOS image sensor for proposed prediction scheme.

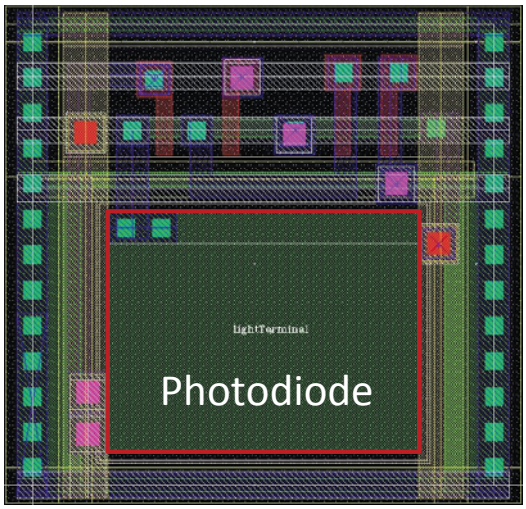


Figure 4.6: The layout overview of a 4-T pixel.

TX, RST, RSL control signals. In the layout, it has four horizontal routing (metal 2, white) and two vertical routing (metal 3, yellow). One yellow wire at the right side represents the column bus, the other one represents the power VDD as well as one white wire connected to it, then the left three white wires represent three digital control signals.

As shown in Figure 4.5, the reset value at FD node is sampled into C1 first, then the diode value at FD node is sampled to C1 again after pixel charge transfer. The difference between them subtracted by CDS is the pixel output without reset noise, and it is sampled and sent for SAR ADC quantization after CDS. The quantized digital data are bit-parallel written into MEM 1 during A/D conversion, next to be bit-parallel written into MEM 2 after A/D conversion. When the operations of one row by column-parallel CDSs and ADCs are complete, the MEM 1 is refreshed to store data from next row data, and MEM 2 still keeps the quantization results of previous row for prediction of the next row.

4.2.2 Memory Circuitry

According to architecture of the CMOS image sensor presented in Figure **??**, MEM1 is used to store fresh quantization values and scan them out and MEM 2 is used to store

historical quantization values. The memory bank of MEM 2 is comprised of a group of latches. The memory bank of MEM 1 is comprised of few DFF shift register chains, which works as not only storing components, but also read-out circuitry. The proposed design is illustrated in Figure 4.7, where the D flip-flops (DFFs) are used to compose shift register chains. The DFFs are used as storing components, and the shift register chains formed by those DFFs are used to shift stored values out one by one.

One DFF shift register chain only stores one type of digital bits from pixels in one row, so there are nine DFF shift register chains are implemented for a 9-bit SAR ADC system in an image sensor. As shown in Figure 4.7, the number of DFFs in one shift register chain is defined by the number of column in a pixel array. When the quantized digital bits are written into DFFs, neighboring DFFs remain unconnected and the inputs of DFFs are connected to output of SAR ADCs. After the quantized values are written into the memory, the neighboring DFFs remain connected to compose shift registers chains to scan the digital bits out one by one. In a word, if this type of memory is implemented in an image sensor with M(row) $\times$ N(column) pixel array and a L-bit ADC system, the memory consists of L N-bit parallel-in and serial-out (PISO) shift register chains (L is ADC resolution). This architecture simplifies the complexity of circuitry by combining storing and read-out, though consumes higher power compared with the static random access memory (SRAM) which is also widely used in CMOS image sensors.

4.3 Column-Parallel SAR ADC Design

4.3.1 Proposed SAR ADC System

The operation principle of SAR ADCs using the prediction scheme is described in this section in detail. Figure 4.8(a) shows the simplified block diagram of the proposed SAR ADC system. The predicted MSBs for a selected pixel are generated using the com-MSB

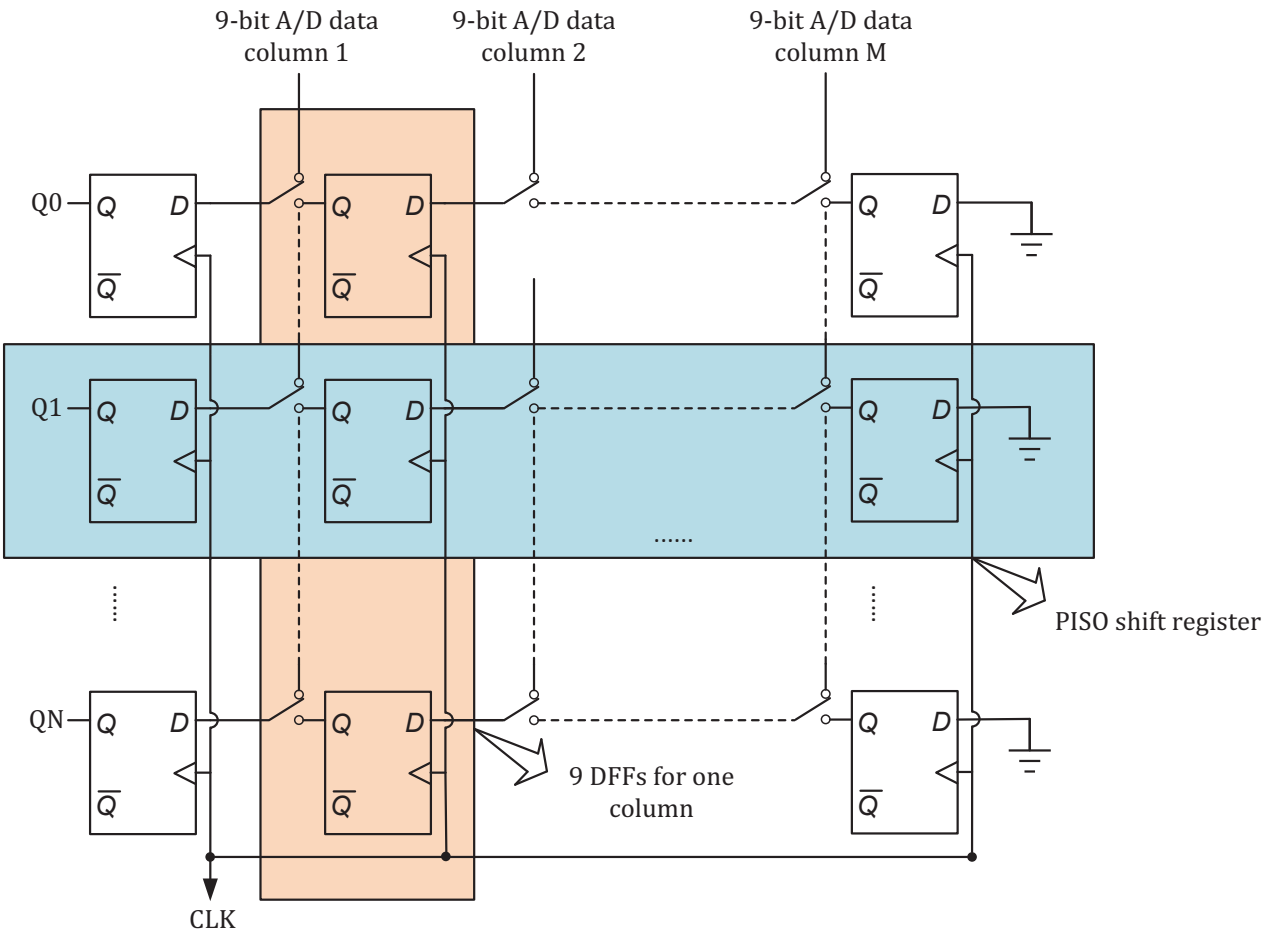


Figure 4.7: Topology of D Flip-Flop chain implemented in memory bank (MEM1).

generator firstly. Secondly, the MSBs are written into DAC to obtain the starting voltage reference, and the quantization values of left bits are obtained by conventional A/D conversion steps. Finally, the correctness of final quantization values is determined using the correct-estimation detector. If it is an incorrect estimation, the correct-estimation detector outputs a signal to reset the com-MSB generator and SAR control logic. The incorrect quantization values are discarded and the SAR ADC restarts a complete A/D conversion. Otherwise, SAR ADC operation of the analog input is complete and quantization values are saved in memory. As shown in Figure 4.8(a), only two more digital logic blocks are internal, com-MSB generator and second-round detector, besides the circuit blocks of a SAR ADC. It has minimum effect on the original ADC after incorporating the prediction scheme, like its linearity, resolution and effective number of bits (ENOB), etc.

The circuit architecture of the DAC implemented in proposed SAR ADC system is presented in Figure 4.8(b). It is a 9-bit split-capacitor array DAC having 48.05 unit capacitors (C) in total. The maximum equivalent load capacitor observed between top and bottom plate capacitor array is 32 C, so the power consumption for SAR DAC and the silicon array is greatly reduced compared with the conventional topology (discussed in Chapter 3). The capacitor array is split into 5-bit MSB and 4-bit LSB array, where the last dummy LSB bit (S0 shown in Figure 4.8(b)) is reported as checking bit. The capacitance of it is one unit capacitance which is same as capacitor of LSB (S1). It does not remain connected to the lower voltage reference (V_{Low}) in the proposed design, and its quantization value is not reported as A/D quantization output. The quantization values of the checking bit and S1 are different, if the prediction is correct, as discussed in Section 4.1. Otherwise, their values are the same.

The architecture of the 9-bit split-binary capacitive DAC is described in Figure 4.8(b), without any extra capacitor accumulated. When the prediction scheme is utilizing in the

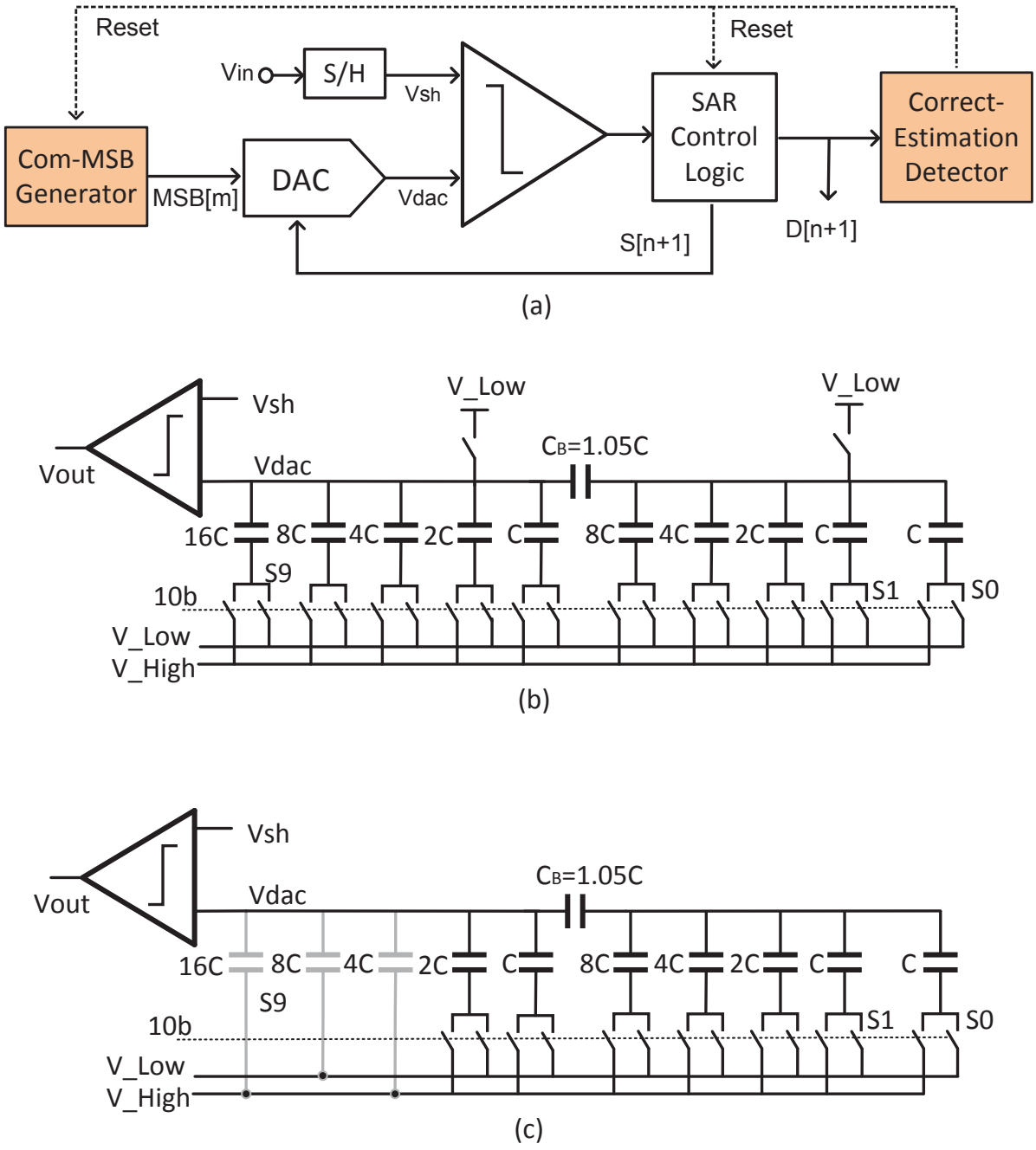


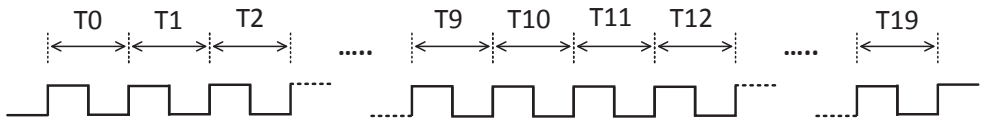
Figure 4.8: (a) Block diagrams of the proposed column-parallel SAR ADC. (b) Circuit architecture of the SAR DAC with comparator. (c) Circuit architecture of SAR ADC with 3-b Predicted MSBs (example shown in Figure 4.2) 101XXXXXX. (The capacitor in first 3 bits are not counted inside SAR control logic operation)

ADC, the predicted MSBs are assigned into the DAC before A/D conversion steps. As shown in Figure 4.8(c), the first three capacitors (16C, 8C, and 4C) are preassigned to 101 after initializing all the capacitors, if the predicted MSBs is 101XXXXXX. Those capacitors are excluded from the A/D quantization steps, and the switching energy consumed by fist three capacitors in a complete A/D conversion cycle is also neglected. The larger the capacitance the larger the switching energy consumed and the total capacitance of first three capacitors is almost twice of left capacitors. This prediction therefore has significant saving in switching energy, as their large capacitors are kept sleeping in A/D conversion cycles.

Overview the architecture of this proposed SAR ADC, no extra capacitor is added on inside and the complexity of entire system is minimized. In order to minimize the parasitic cause by C_B (as discussed in Chapter 3), the unit capacitor is set a slight large instead of introducing the calibration circuitry inside ADC system. The calibration circuitry has complex architecture and is area consuming, which is hard to merge it with a column ADC system whose layout pitch size is quite small. The moderate resolution of this ADC system also makes it be acceptable for this image sensor topology, even though without a calibration circuit implemented inside.

4.3.2 Timing Diagram of SAR ADC

The operation procedures of the proposed SAR ADC, following with clock cycles, are illustrated in Figure 4.9. The first cycle T0 is used to generate com-MSBs and assigned the predicted MSBs value for an analog input before ADC conversion. T1 to T9 are 9-bit SAR ADC conversion cycles, where the conversion cycles corresponding to the predicted MSBs are useless, and the left cycles are used for A/D conversion of left bits. T10 is used for A/D conversion of checking bit (S0 shown in Figure 4.8), which is used to determine the correctness of the predicted MSBs. If the predicted MSBs estimated are incorrect,



T0 : Preset the (m-1) bits common-MSB into DAC
T1—T9 : Successive Approximation Conversion
(If there are 4b common MSBs preset into DAC, then only T5 to T9 are used, and ADC use the 4b common-MSB during T1 to T4)
T10 : Determine the correctness of prediction scheme
(If S_dum has same value as S0, it is wrong estimation; otherwise, it is correct estimation.) (Refer to Fig. 3)
T11—T19 : Another Successive Approximation Conversion
(If it is incorrect estimation, T11 to T19 are used for another A/D conversion cycle; otherwise, T11 to T19 are not used.)

Figure 4.9: Conversion cycles of SAR ADC using proposed control logic.

another 9 cycles (T11 to T19) are assigned for a new SAR A/D conversion cycle to generate the accurate quantization values. Otherwise, T11 to T19 are not used and final quantized digital bits together with predicted MSBs are temporarily saved in memory. When the correct quantization results are obtained and saved in memory, the pixels in the next row are processed using the same methodology with the SAR ADCs.

4.3.3 Design of Comparator

The proposed SAR ADC system uses a latched-type comparator with a preamplifier [11]. The schematic is presented in Figure 4.10, where the pre-amplifier is a single-pole, one-stage amplifier and the latch is a static latch. The total offset of this comparator is illustrated as follow:

$$V_{off_T}^2 = V_{off_amp}^2 + \frac{V_{off_latch}^2}{A_{preamp}} \qquad \text{(Eq. 4.1)}$$

The configuration of this comparator benefits from low input-referred offset and thus is able to detect small voltage difference at its inputs. According to Eq. 4.1, the input

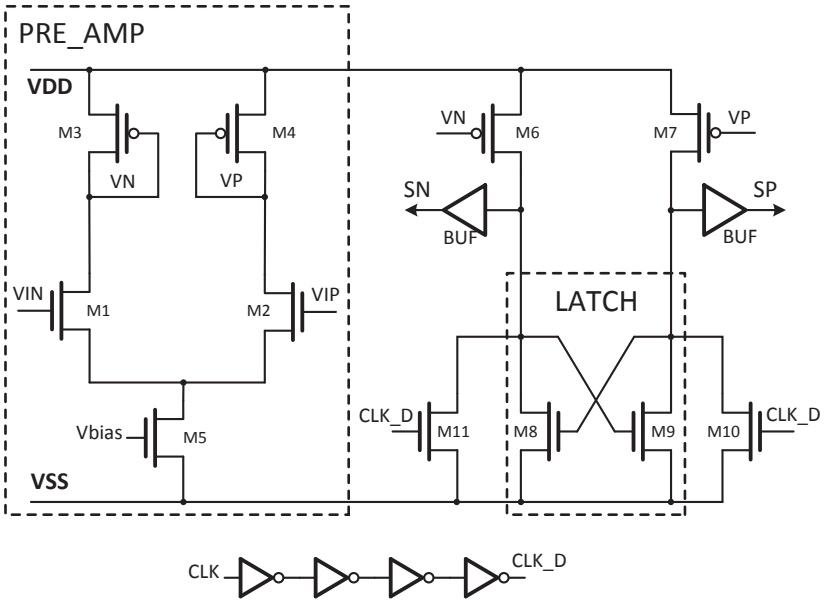


Figure 4.10: Comparator schematic including latch and pre-amplifier.

Table 4.1: Specifications and simulation results of pre-amplifier

	M1,M2	M3, M4	M5	Vbias [V]	A_{vdB} [dB]	f_{-3dB} [MHz]
Size of MOSFET	1/10	1/1	1.5/2	0.8		
Pre-amplifier					35.84	41.7

referred offset, a much lower offset voltage at the input is obtained by increasing pre-amplifier gain. The speed of this comparator is reduced by increasing the gain, so the speed-gain trade-off exists for this type of comparator.

In the proposed CMOS image sensor, the clock frequency is 20MHz which is a moderate speed. So a high gain pre-amplifier is designed according to the speed-gain tradeoff. The design specifications of the pre-amplifier is summarized in Table 4.1. It shows that this pre-amplifier tense a very high gain but a moderate bandwidth, resulting that the comparator has a smaller input referred offset but moderate speed.

Table 4.2: Size setting of Latch

	M6,M7	M8,M9	M10,M11
Size of MOSFET	6/2	3/3	1/1

Figure 4.10 shows the architecture of a latched comparator, where the right side is the static latch. It is comprised of two NMOS transistors, M8 and M9, which compose a positive feedback to accelerate the speed of comparison. Transistor M6 and M7 are connected with M3 and M4, forming two current mirrors. Initially, the currents mirrored from pre-amplifier are sent to the latch. In the next step, the difference between them are differentiated by the positive feedback of the latch, until the higher one reaches the maximum value (VDD) and lower one reaches the minimum value (VSS). Finally, the stabilized voltages at regeneration nodes of M6 and M7 are comparison results which are buffered as the outputs of comparator by digital buffers. Transistor M10 and M11 are used to reset the latch to lowest voltage level (VSS) before comparison, and the reset signal is defined by clock signal. The clock signal after being delayed by four invertors is utilized to comparator, which is used to send out the comparison results at the same time that they are captured by the successive approximation register. Because the comparison results passing into DFFs of successive approximation register is slightly delayed by the inherent delay of DFF chains, when the system operates with universal a clock signal. The transistor sizes of transistor in latch side are summarized in Table 4.2.

4.4 Simulation and Testing Results

4.4.1 Simulation

4.4.1.1 Capacitor Switching Energy Analysis

Based on the spatial likelihood feature of most natural scenes and operation principle of prediction scheme, the predicted MSBs are most estimated correctly in natural scenes. In other word, it means that he switching energy consumed by A/D conversion steps of those MSBs are neglected, with the purpose of reducing the power consumption of an ADC system, even a CMOS image sensor. The capacitor switching energy analysis for a 9-bit split-capacitor array DAC (as shown in Figure 4.8) is analyzed in this section. With

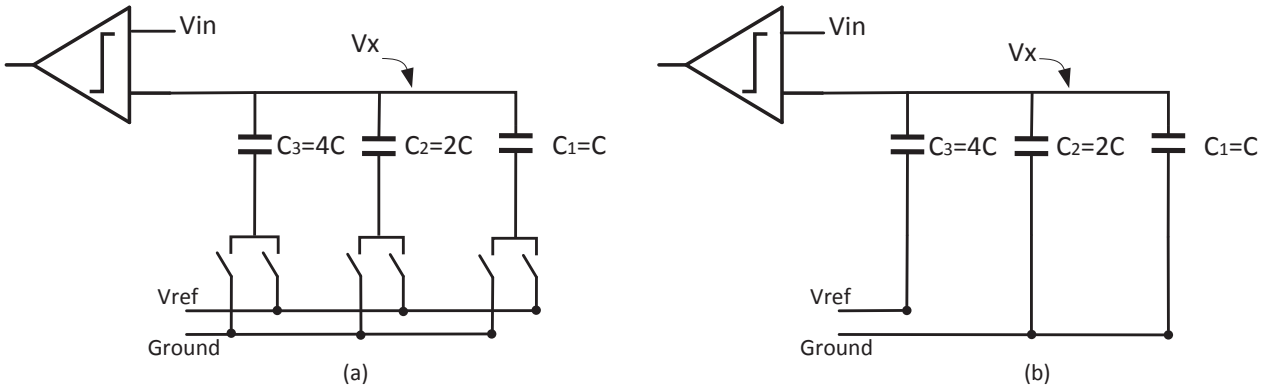


Figure 4.11: 3-bit ADC capacitor (a) array and (b) array for the 1st step switching method.

purpose of easy explanation, the methodology of calculating capacitor switching energy is explained based on architecture of a 3-bit capacitive DAC shown in Figure 4.11. The capacitors are initialized before A/D conversion, where both the bottom and top plates of the capacitors are connected to Ground. At time 0, the bottom plate of capacitor C_3 is connected to V_{ref} and the capacitor array is charged. At time 1, the final value is 1/2 V_{ref} at top plate based on the charge conservation theory presented in Chapter 3.

The total energy drawn from V_{ref} is:

$$\begin{aligned} E_{0->1} &= \int_0^1 i_{ref}(t) V_{ref} dt \\ &= V_{ref} \int_0^1 i_{ref}(t) dt \end{aligned} \qquad \text{(Eq. 4.2)}$$

where $i_{ref}(t) = -\, dQ_{C_3}$, $Q_{C_3} = 4CV_x[0]$,the Eq. 4.2 is simplified to:

$$\begin{aligned} E_{0->1} &= -V_{ref}\int_0^1 (dQ_{C_3}/dt)dt \\ &= -V_{ref}\int_{dQ_{C_3(0)}}^{dQ_{C_3(1)}} dQ_{C_3} \\ &= -V_{ref}(Q_{C_3(1)} - Q_{C_3(0)}) \\ &= -V_{ref} * 4C * ((V_x(1) - V_{ref}) - V_x(0)) \\ &= 2C * V_{ref}^2 \end{aligned} \quad \text{(Eq. 4.3)}$$

The up/down movement of second step is decided comparison result D_1 at first step. If D_1 is 0 (means $V_{in} > V_x$), the C_3 remains connected to V_{ref} and C_2 is connected to V_{ref} as shown in Figure 4.12(a). The V_x[i] shown in this example is used to indicate the voltage on the top plate of this capacitor array in i_{th} A/D conversion step. At time 2, V_x[2]=3/4 V_{ref}. The total energy drawn from V_{ref} for an "up" transition is computed as follows:

$$\begin{aligned} E_{1->2,up} &= -V_{ref}[4C((V_x[2] - V_{ref}) - (V_x[1] - V_{ref})) + 2C((V_x[2] - V_{ref}) - V_x[1])] \\ &= (1/2)CV_{ref}^2 \end{aligned} \quad \text{(Eq. 4.4)}$$

In terms of "down" transition, the C_3 remains unconnected to V_{ref} and C_2 is connected to V_{ref}. At time 2, V_x [2]=1/4 V_{ref} after the charge in capacitors is stabilized, as shown in Figure 4.12(b). The total energy drawn from V_{ref} for an "down" transition is computed as follows:

$$\begin{aligned} E_{1->2,down} &= -V_{ref}[2C((V_x[2] - V_{ref}) - V_x[1])] \\ &= (5/2)CV_{ref}^2 \end{aligned} \quad \text{(Eq. 4.5)}$$

According to the analysis of switching energy in a 3-bit DAC, the total switching energy consumed by a 9-bit split-capacitor array DAC system can be calculated. Figure

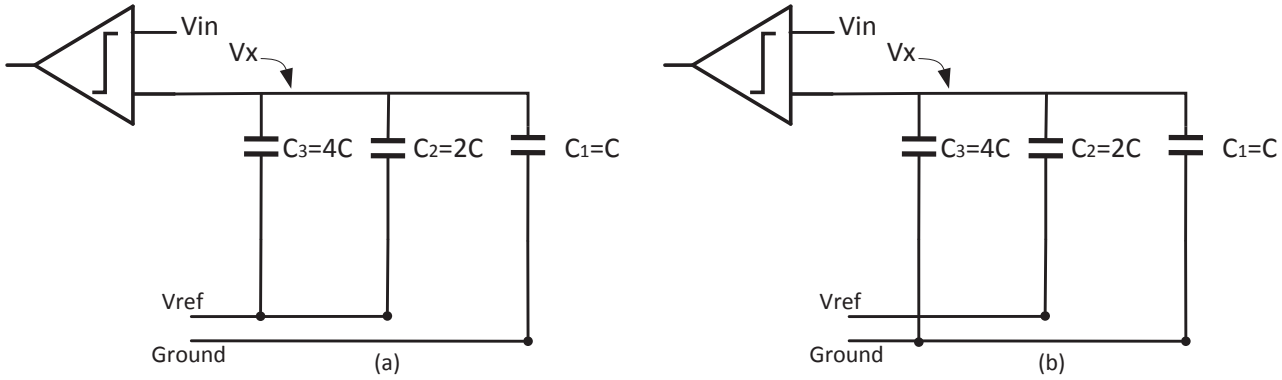


Figure 4.12: 3-bit ADC capacitor (a) array and (b) array for the 1st step switching method.

4.13 shows the switching energy distribution curves versus the ADC output code, based on the prediction scheme. Series1 represents the case of a 9-bit split-capacitor array DAC without any predicted MSBs assigned. Series 2 to 9 represent the switching energy curves for a 9-bit split-capacitor array DAC with the number of predicted MSBs varying from 1 to 8. The figure shows that the switching energy is significant reduced if number of predicted MSBs is larger. In order to analysis the switching energy saved for this architecture of DAC, the average switching energy of 9 Series and the percentage saved of them compared with Series 1 are illustrated in Table 4.3. The switching energy is saved more obviously when the number of predicted MSBs is 1 or 2, as first two MSBs are the highest weighted capacitor in the capacitor array.

Two reference voltages are assigned for the SAR ADC in the hardware design, the V_{ref} assigned for switching energy calculation is changed to ΔV_{ref}=(V_{refH}-V_{refL}), where V_{refH} and V_{refL} are upper/down limits of the reference window. As there are two cases (correct and incorrect prediction) for the prediction scheme, the estimated switching power per conversion cycle of the DAC is calculated as follows:

E_{total} = E (a 9b conversion with m bits predicted MSBs) ← Correct Prediction;

E_{total} = E (with m bits predicted MSBs) + E(a 9bit conversion) ← Incorrect Prediction.

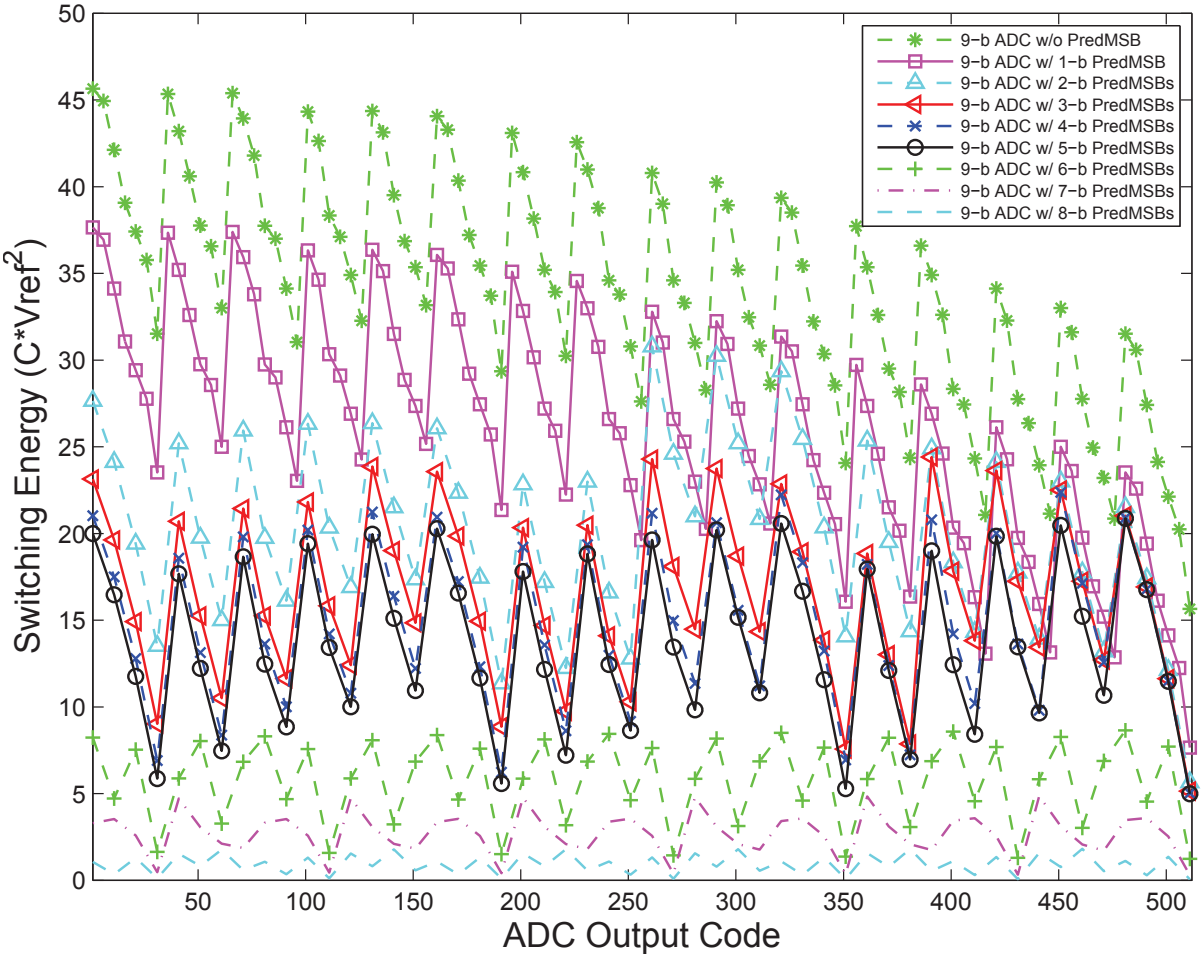


Figure 4.13: The Average Switching Energy Per Conversion For Different Bit

Table 4.3: The Average Switching Energy Per Conversion For Different Bit

Predicted MSBs (m bits)	Average Switching Energy (E_{ave} ($C*V_{ref}{}^2$)	Saved Switching Energy comparing to 0 predicted MSB case
0	34.103	0%
1	26.103	23.4584%
2	20.103	41.0522%
3	16.603	51.3153%
4	14.728	56.8133%
5	13.759	59.6540%
6	5.7670	83.0895%
7	2.7064	92.0640%
8	0.9413	97.2399%

4.4.1.2 System Simulation Results

According to the switching energy analysis above, several groups of natural images are taken into MATLAB simulation. The MATLAB simulation setup is illustrated in Figure 4.14, where the pixel values in digital mode are obtained first for an input image. Then the predicted MSBs for pixels in second row (as no prediction utilized in first row) are estimated. A checking step is used to check the correctness of predicted MSBs: If predicted MSBs are correct, the conversion steps is (N-m) steps and switching energy is switching energy of a 9-bit A/D conversion with m-bit predicted MSBs. Otherwise, the conversion steps is (2N-m), and switching energy is composed of a 9-bit A/D conversion with m-bit predicted MSBs and a 9-bit ADC without any predicted MSBs.

The same operating route is repeated for next row until the last row of pixel array, and the total conversion steps and switching energy are calculated after that. The total conversion steps and switching energy saved are estimated by comparing total conversion steps and switching energy consumed in an imaging system with prediction scheme and one without prediction scheme.

As shown in Figure 4.13, the first group of images is obtained from a standard image library, which is popular used in image processing field. Another two groups of pictures

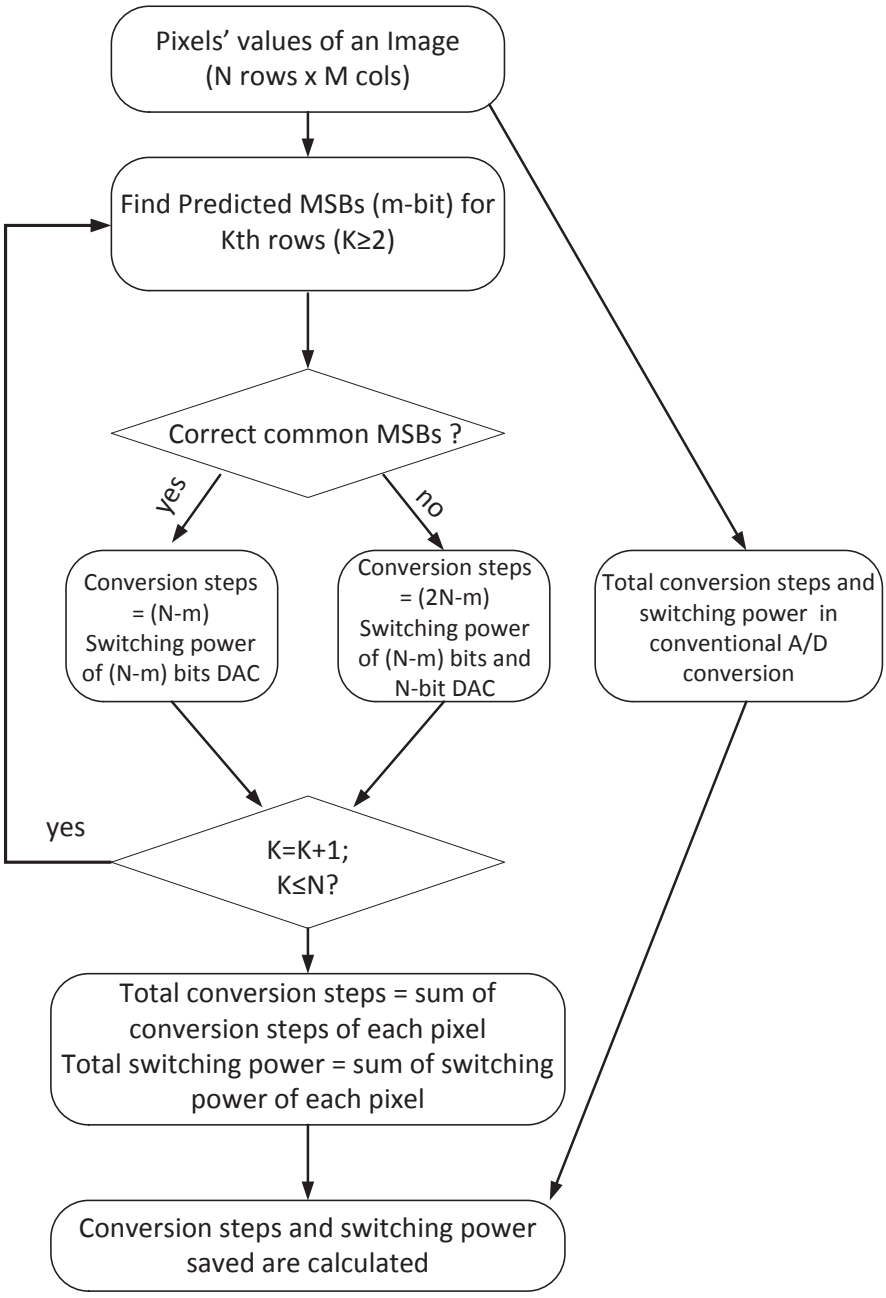
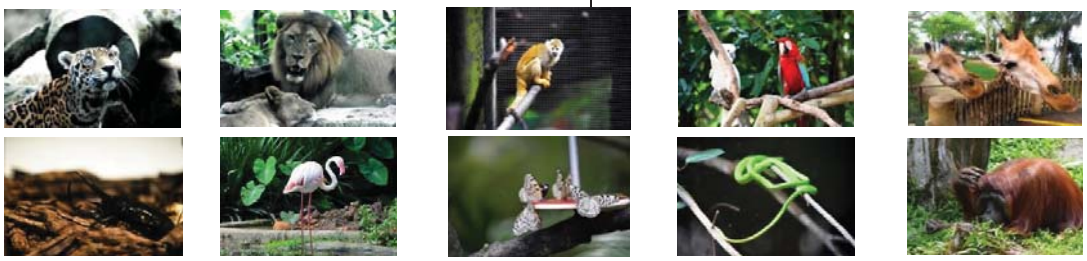


Figure 4.14: Calculation procedures on calculate the conversion steps and switching energy saved for an image using Matlab.

Standard Test Image (http://www.imageprocessingplace.com/root_files_V3/image_databases.htm)

Averaged Conversion steps Saved	21.44%
Averaged Switching Energy Saved	21.02%

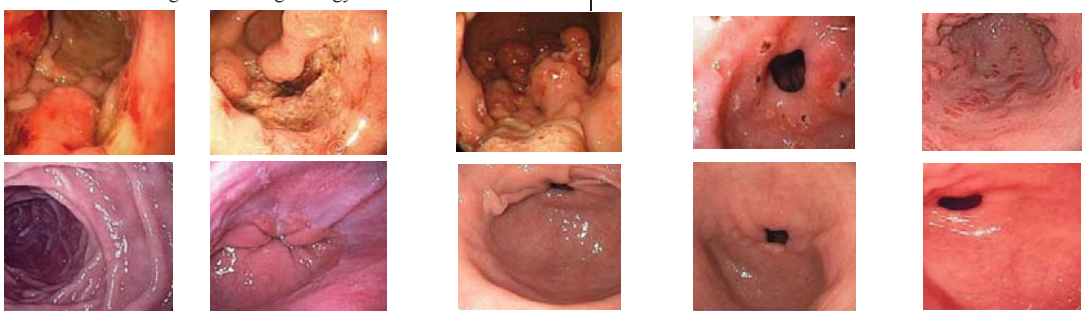


Images taken at Singapore Zoo

Averaged Conversion steps Saved	25.66%
Averaged Switching Energy Saved	29.07%

Images taken at Venice, Italy

Averaged Conversion steps Saved	27.74%
Averaged Switching Energy Saved	31.16%



Inner views of stomach and intestine.

Averaged Conversion steps Saved	31.04%
Averaged Switching Energy Saved	32.50%

Figure 4.15: Total conversion steps and switching energy saved based on common-MSBs of previous-row compare to the conventional SAR for four groups of pictures.

are taken at Singapore zoo and Venice, Italy respectively, which are natural images. The last group of images shows the inner view of stomach and intestine, which is obtained from internet. During simulation, the total A/D conversion steps and switching energy of an image are calculated based on prediction scheme, and the saving on both aspects are estimated by comparing with the total steps and switching energy consumed in a conventional imaging system. as well as the switching energy saved. The averaged values of savings on both aspects for those groups of images are listed in Figure 4.13. It shows that up to 10% to 30% saving on total conversion steps, and 20% to 30% saving on switching energy for most of images. The switching energy saved is more obvious for last group of images, as the inner views of stomach have higher similarity in pixel values.

4.4.1.3 ADC Simulation

Based on the architecture of the proposed SAR ADC system, it consists of two additional circuit blocks besides of the architecture of a conventional SAR ADC. In the hardware implementation, a CMOS image sensor with column-parallel SAR ADCs was fabricated, without fabricating an individual SAR ADC. The performance of SAR ADC system with additional circuit blocks and the prediction scheme would not be measured. The performance of ADC was simulated only and the performance is summarized in Table 4.4. The simulation setup for a SAR ADC is shown below.

- Measuring DNL & INL

  Histogram testing is widely used to determine DNL and INL errors for convertors. The histogram of an ADC shows how many times each different digital code words appear on the ADC output, with a given analog input signal. One method of histogram testing involves the sampling and digitizing of a slow (with respect to conversion time) single-slope ramp signal as shown in Figure 4.16. The voltage boundaries of this ramp are defined by the input range of the ADCs, and the time

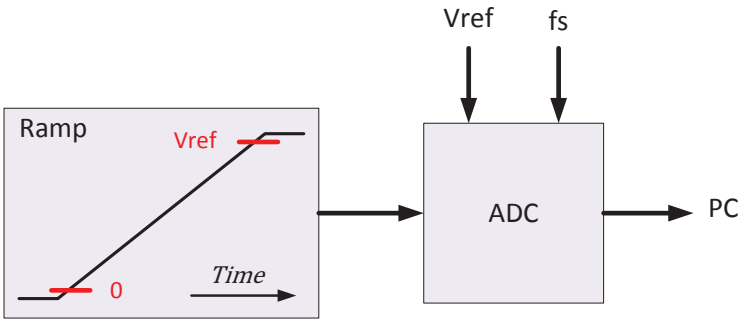


Figure 4.16: Histogram simulation setup.

period of entire ramp (0 to V_{ref}) is defined by ADC conversion time, resolution of ADC, and how many times of digitizing action for one digital code.

$$Time = T_{ADC} * 2^N * m \quad \text{(Eq. 4.6)}$$

where T_{ADC} is the ADC conversion time for an given analog input, N is the resolution of ADC and m is the digitizing times for each digital code word. So for this proposed design, 9-bit ADC with 50-points histogram test, the time for this linear ramp is 12.8 ms. Those ADC outputs generated are saved in a txt file and processed by the Matlab code to calculate the DNL and INL errors. DNL is derived directly from total number of occurrences of each code at the output of the ADC, and the INL is the accumulation of DNL.

- Dynamic Simulation

  As discussed in Chapter 2, the dynamic specifications of ADCs are categorized as SNR, SINAD, ENOB, THD. The direct application of the fast Fourier transform (FFT) is the simplest frequency-domain test widely used in dynamic simulation. During testing, the ADC was driven by a single, low distortion sine wave. The SNR, SINAD, ENOB and THD were easily calculated by taking the FFT of the output data collected from ADC. The simulation setup is illustrated in Figure 4.17, the

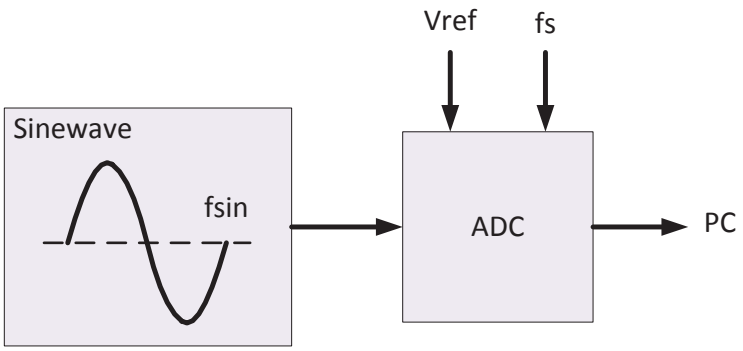


Figure 4.17: FFT simulation setup.

sampling frequency (f_s), the input test tone (f_{sin}) and the size of the data record (N_{record}) should be precisely selected. The f_s is the sampling frequency of ADC determined by the SAR ADC, the N_{record} is the number of data points which is greater than 2^N, where N is the resolution of ADC. The optimum input test town occurs when the N_{record} distinct phased sampled are uniformly distributed between from 0 to 2π radians. Taking this knowledge into account, the coherent sampling is described as sampling of a periodic signal, where an inter number of its cycles fit into a predefined sampling window. The input test tone is expressed as:

$$f_{sin} = (N_{window}/N_{recorded}) \times f_s \qquad \text{(Eq. 4.7)}$$

where the N_{window} is an inter number of cycles whin the sampling window mentioned above. The f_s = 2MHz and the $N_{recorded}$ is chosen as 1024 point for the proposed 9-bit ADC. The N_{window} has to be an integer odd or mutually prime number for a 1024-point data record $N_{recorded}$, the final/near-optimum input test tone is calculated as follows:

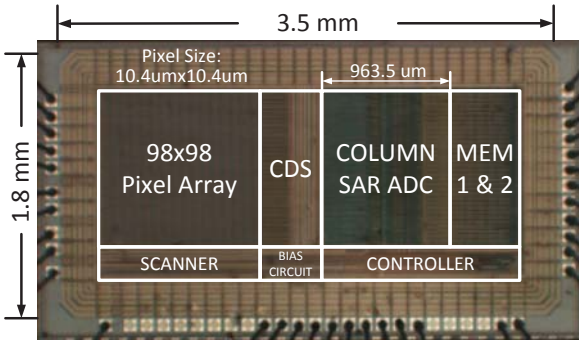


Figure 4.18: Chip microphotograph. Die size is 3.5 x 1.8 mm^2.

$$f_{sin} = (N_{window}/N_{recorded}) * f_s$$
$$f_{sin}(\text{mutually prime}) = (1021/1024) * 2MHz = 1.994MHz \quad \text{(Eq. 4.8)}$$
$$f_{sin}(odd) = (1023/1024) * 2MHz = 1.998MHz$$

The frequency of the sine wave was set as 1.994MHz during FFT testing of dynamic performance of ADC. Those ADC output values were used to calculate the dynamic specifications through Matlab codes.

4.4.2 Testing

A CMOS image sensor with the column-parallel SAR ADC system implementing with the proposed prediction scheme was fabricated using 0.35μm AMS CIS (2P4M) technology. The die micrograph of fabricated sensor chip is shown in Figure 4.18 where the die size is 3.5x1.8 mm^2. The pixel array is 98x98 with pixel size 10.4x10.4μm^2, and the length of column SAR ADC is 963.5μm.

As the column parallel ADCs are implemented in the image sensor, the input/output signals of this CMOS image sensor are easily figured out, as shown in Figure 4.19. At the output block diagram, the 9-bit quantization digital codes from the column-level ADCs are always scanned out after the pulse of write data signal in output block. At

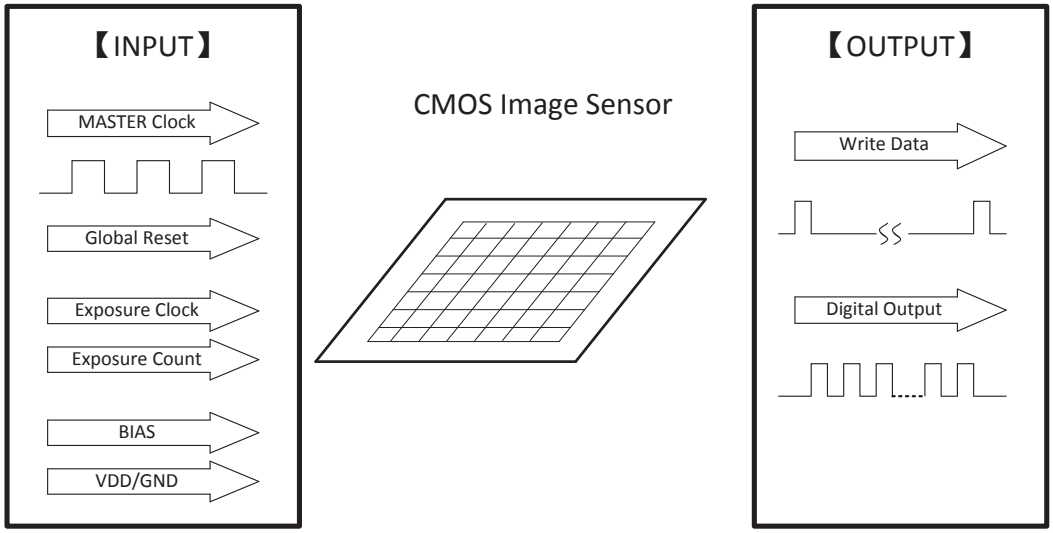


Figure 4.19: CMOS image sensor Input/Output block diagram.

the input block diagram, there are two clock signals: the exposure clock is used only for the exposure counter and the master clock is used in the entire digital system of the image sensor. The exposure counter can be programmed to set the exposure time using the values of input exposure count and exposure clock, according to the lighting environment. The global reset is the enable signal of imaging system, which is used to initialize the entire system to do exposure, quantization and readout. The bias signals are three reference voltages utilized for CDSs and ADCs shown in Figure 4.18, where one bias is used as reference voltage for op-amps of CDSs and other two bias are used as reference window of SAR ADCs. The power supplies for the imaging system are divided into three groups: the first group is used for the pixel array, the second group is used for digital circuitry, and the last group is used for analog circuitry. For the purpose of isolating the effects caused by different circuit domains.

4.4.2.1 Testing Setup

In order to simplify the hardware to provide the input signals and collect the output signals of the image sensor , a FPGA board with Opal Kelly is implemented for testing

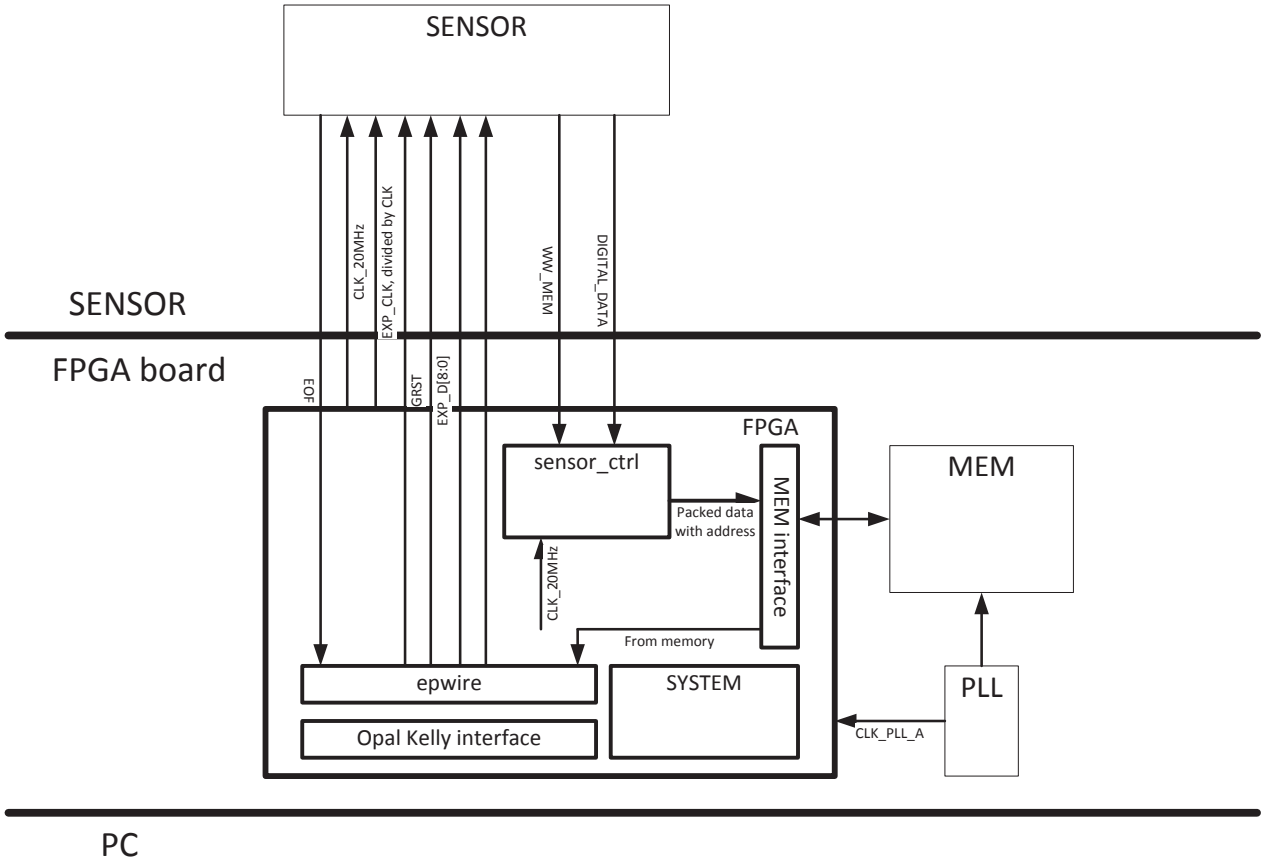


Figure 4.20: Block diagram of testing platform for a CMOS image sensor.

the image sensor shown in Figure 4.21. The block diagram of testing platform with FPGA board is illustrated in Figure 4.20, where the FPGA board is the bridge link the Sensor and PC together. The FPGA board consists of the FPGA (Field Programmable Gate Array), SDRAM and PLL (phase locking loop). The FPGA includes blocks of sensor controller, memory interface, Opal Kelly interface, etc. This board provides the digital signals required by image sensor. It also receives the output signals from sensor and transfers them to PC. The PLL is used to generate the different clock signals required in the imaging system, and the MEM (memory) is used to store the digital outputs.

When hardware is set up, the software coding is used to build up a virtual hardware model to connect the sensor and FPGA, FPGA and MEM, PLL and FPAG, as well as the communication interface between PC and FPGA board. The software coding contains

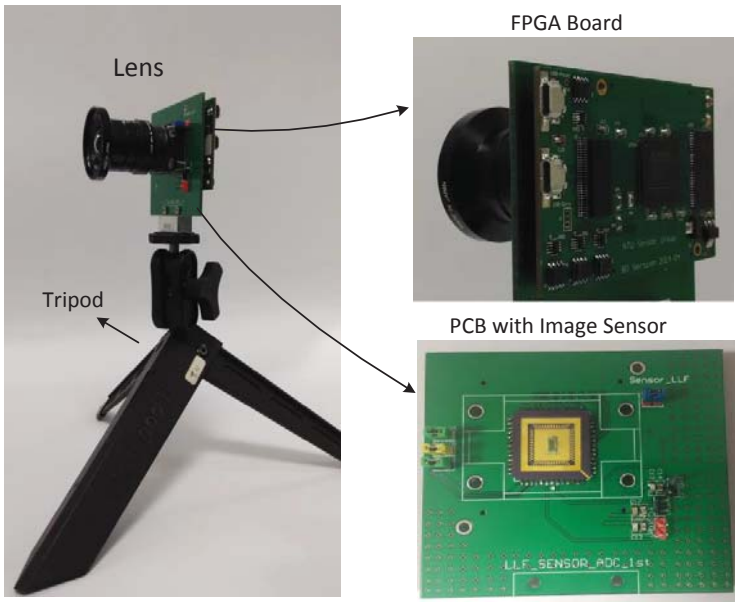


Figure 4.21: Hardware Setup for Testing.

two parts: one is hardware description language (Verilog), which is used to build the virtual hardware model. This virtual hardware model provides the digital control signals required by image sensor. It also generates those digital signals same as those produced in image sensor (shown in Figure 4.19), in order to debug whether they are generated correctly or not. The other one is C++ coding which is used to build the communication interface between PC and FPGA board. A GUI (graphic user interface) is also built to visualize the sensor function and display the images.

The testing setup of the CMOS image sensor is shown in Figure 4.21, where presents two PCB boards. One is FPGA board which works as small CPU to program the digital control signal required by imaging system and output the digital data to PC. The other one is the PCB with image sensor, which only contains a CMOS image sensor and some capacitors decoupling for the power supplies. As the image sensor is a system-on-chip (SoC) product, and its outputs are converted to digital code already. The lens is used to capture the picture from real world, which is normally not used when testing the

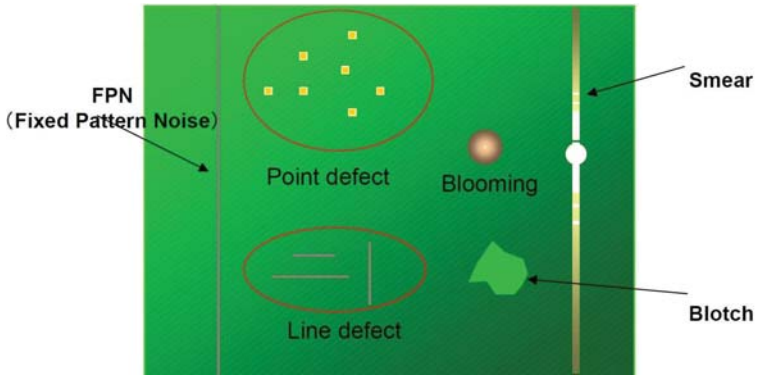


Figure 4.22: Defects of an image.

performance of sensor in dark room. The clocks and bias signals are generated by FPGA board as shown in Figure 4.20, so their performances are not included in the testing list of the image sensor.

The characterizations of testing a CMOS image sensor are categorized into three parts: (1) Digital logic test: the critical test items include continuity, short, input leakage and power consumption. Since the digital logic was not designed to be insulated from the whole system for testing, so only power consumption was tested. (2) ADC function test: the critical test items are SNR, linearity and ENOB. As the SAR ADC was implemented with a prediction scheme which introduced addition circuits and processing steps insides. The simulation of the ADC is explained in section 4.4.1.3 and summarized in Table 4.4. (3) Image performance test: the critical test items contain dark current, sensitivity, fixed pattern noise (FPN), dynamic range (DR), etc. Figure 4.22 shows the FPN, point defect, line defect, blooming, smear and blotch of an image. The image performance testing is illustrated below,

- FPN Test

  FPN is the spatial variation in pixel output values under uniform illumination due to device and interconnect parameter variations (mismatches) across the sensor. It

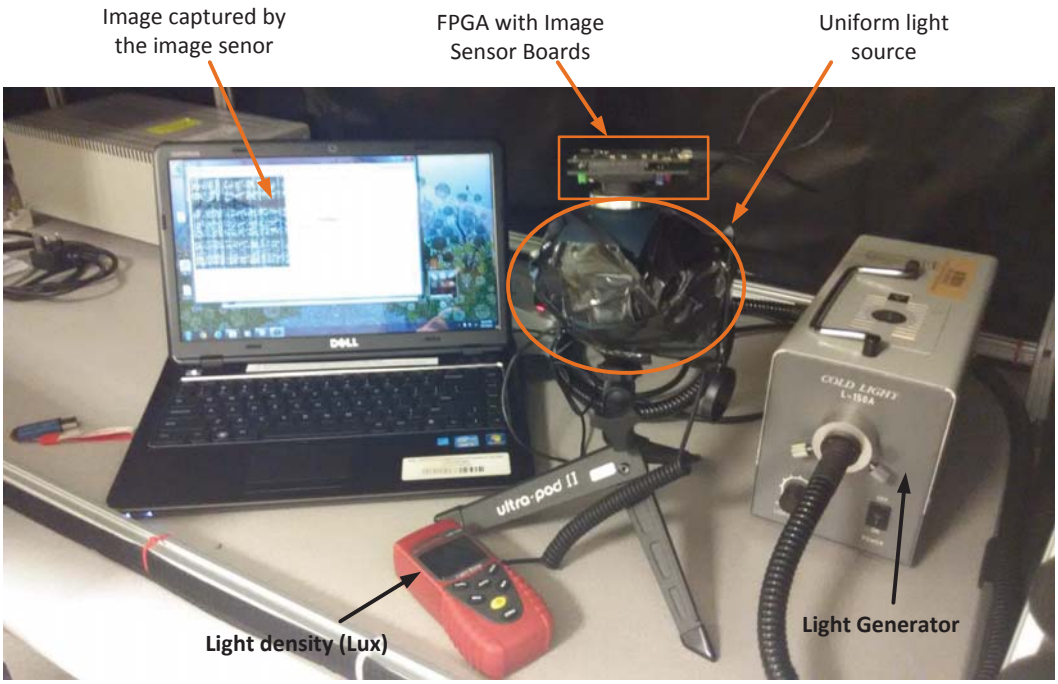


Figure 4.23: Setup of image performance testing.

is normally fixed for a given sensor, but varies from sensor to sensor. So if v_0 is the nominal pixel output value at uniform illumination, and the output pixel values (excluding temporal noise) from sensor are v_{ij} for $1 \leq i \leq n$ and $1 \leq j \leq m$ (where $n \times m$ is the resolution of a given image sensor), then the FPN is estimated as values $\Delta v_{0ij} = v_{oij} - v_0$. FPN is typically reported as the standard deviation of the spatial variation in pixel outputs under uniform illumination as a percentage of voltage swing.

In order to measure the FPN due to different device parameters, the image sensor is used to take many frames under uniform illumination. The testing setup is illustrated in Figure 4.23, where the light source is used to provide the uniform illumination to the sensor, and the light density is decided by the controller. Frames are captured by the sensor and quantization values are sent to PC for image reconstruction. When the sensor is capturing frames, the light density remained

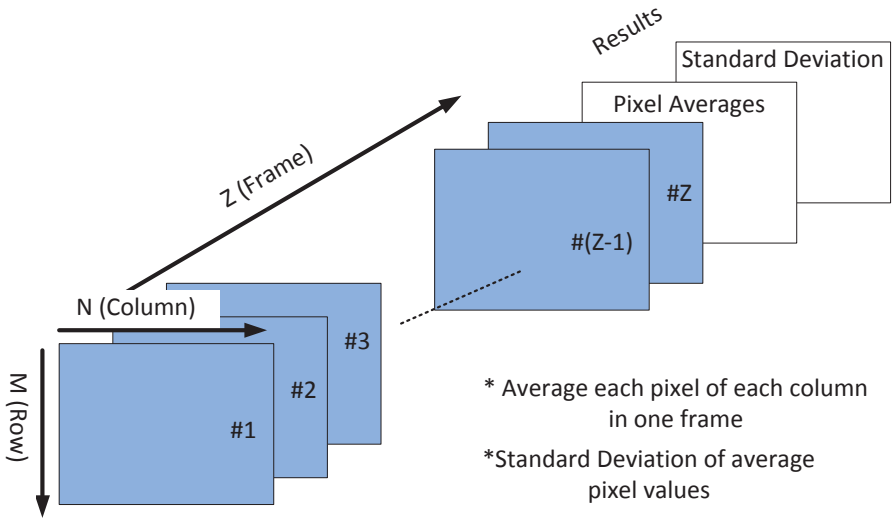


Figure 4.24: Frame processing of calculating FPN.

moderate and kept as same, as well as the exposure time. So if Z (for example Z=100) frames with the same illumination were taken shown in Figure 4.24, all the pixel values of each column in one frame were averaged and the $Z * N$ pixel averages were obtained. The standard deviations of those averages were calculated cross frame, as well as the averages of all averaged pixel values. The value of pixel FPN is calculated as the standard deviation over the final average value.

$$\text{FPN} = \frac{\text{Standard Deviation}}{\text{Average Pixel Value}} = \frac{\sigma}{V_{ave}} \qquad \text{(Eq. 4.9)}$$

- Sensitivity Test

  The sensitivity is defined as the ratio of output signal [V] to an incident illumination level [lux] in a second. The unit of sensitivity is [V/luxs]. Sensitivity is reported as the mean value or color ratio of an image, and the mean value test is applicable to the implemented CMOS image sensor to calculate sensitivity as color filter was not implemented in sensor. Frames (the number of frames is Z=50) are taken under uniform illumination by the image sensor as shown in Figure 4.23, and average all the pixel values in voltage domain. The sensitivity is calculated as:

$$\text{Sensitivity} = \frac{\text{Average Voltage}}{\text{Exposure Time} * \text{Illumination}} \quad \text{(Eq. 4.10)}$$

- Dark Current Test

  The dark current is defined as a leakage current of a photodiode without any illumination, and its value is typically dependent on the process. In order to analyze the dark current, the same methodology used in FPN test is implemented. The testing setup is same as FPN measurement shown in Figure 4.23, in complete dark condition. The same number of frames are taken by the image sensor with same exposure time and zero light illumination, the average values of each pixel over N frames are calculated and the dark current can be reported as:

$$\text{Dark Current} = \frac{\text{average value of pixels}}{\text{exposure time}} \quad \text{(Eq. 4.11)}$$

- Dynamic Range Test

  Dynamic range quantifies the sensor's ability to adequately image both high lights and dark shadows in a scene. Dynamic range is reported as the ratio of the largest non-saturating photocurrent to the smallest detectable photocurrent, which is typically defined as the standard deviation of the noise under dark conditions. Normally the maximum and minimum current are defined as:

$$\begin{aligned} i_{max} &= \frac{qQ_{sat}}{i_{int}} \\ i_{min} &= \frac{qQ_{readout}}{i_{int}} \end{aligned} \quad \text{(Eq. 4.12)}$$

  The dynamic range is calculated as Eq. 4.13, where the Q_{max} is the full-well capacity and V_{sat} is the signal swing.

Table 4.4: Performance Summary of the Image Sensor

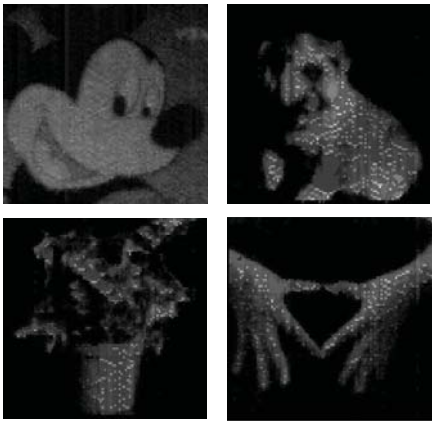
Process Technology	0.35 μm AMS (2p4M)
Chip size	3.5 × 1.8 mm^2
Sensitivity	0.33A/W
Dark current	11mV/s
Dynamic range	44.12dB
FPN	1.24%
Power supply	3.3V
Power consumption	42.3mW
ADC resolution	9 bits
ADC input range	2V
ADC clock frequency	20MHz
ADC DNL/INL	(+0.55,-0.91)/(+1.34/-1.8)
ADC SNR	49dB

$$DR = \frac{i_{max}}{i_{min}} = \frac{Q_{max}}{\sigma_{readout}} = \frac{V_{sat}}{\upsilon_{rms}} \quad \text{(Eq. 4.13)}$$

Where V_{sat} is the signal swing, which is reported as the output range of an image sensor. is converted from the standard deviation by averaging from a number of consecutive frames in the complete dark condition. Those frames captured during dark current testing are utilized in dynamic range testing. The pixel values over frames for the same pixel (pixel(i,j)in the array) are averaged and the standard deviation of them is reported as υ_{rms}. Finally, the dynamic range of the sensor is calculated as 44.12dB.

4.4.2.2 Testing Results

After the testing setup and measurements setup for image sensor, the performances of implemented sensor is measured and summarized in Table 4.4. The total power consumption of this sensor is 42.3mW with 3.3V power supply, sensitivity of the imaging area is 0.33 A/W, duck current is 11mV/s, the dynamic range is 44.12dB and the FPN is 1.24%. In terms of the column-parallel ADCs, voltage reference window is 1V to 3V,



Parameter	Average Saved
D8	84.75%
D7	77.075%
D6	67.9%
D5	56.22%
D4	45.41%
D3	37.695%
D2	32.5425
D1	32.485%
D0	-8.69%

Figure 4.25: Sample image taken by the prototype CMOS image sensor.The total conversion steps and switching energy saved are 47.26% and 76.1% respectively through Matlab simulation.

the clock frequency is 20MHz, the ADC DNL/INL are (+0.55, -0.91) LSB, (+1.34, -1.8) LSB respectively, and SNR of ADC is 49dB.

With testing setup with FPGA board, PC, lens and tripod shown in Figure 4.21, a few sample images are presented in Figure 4.25 taken by the CMOS image sensor. With assumption that the algorithm operation works properly in the hardware, the sample image are processed through the MATLAB simulation to obtain the conversion steps and switching power saved. As shown in Figure 4.21, the average conversion steps saved for each bit is also illustrated in the table, the most saving bit on those nine quantization bit is the first MSB and its value is 84.75%. Because the MSBs are the main contribution to switching power consumption. In terms of all the images, the average savings in total conversion steps and switching energy are 47.26% and 76.1% respectively. The such high saving in the switching energy of this sample image could be concluded as several reasons: the pixel resolution of this prototype image sensor is quite small (98×98); the hardware was not implemented with color filter which simplify the pixel values of a frame; the objects capture by this image sensor are simple; and the dynamic range of image sensor is small which narrow down the variable range of pixels. There are some white dots

appearing in those sample images, which is resulted by the design error in digital circuit. This error caused the pre-saturation during ADC processing for pixel values and it will be solved in next design.

4.4.3 Comparison

Regarding this design, only one CMOS image sensor with the proposed prediction scheme is fabricated. So the comparison with exactly same CMOS image sensor but without prediction scheme is not applicable. The comparison with another SAR ADC with conventional operating methodology is listed in Figure 4.26. The reference [16] taken into consideration is a CMOS image sensor implemented with column-paralle SAR ADCs, where binary-weighted capacitor array DACs with multiple references are implemented inside the SAR ADCs. According to the comparison table, the power consumption of proposed work is 2.115 mW/Mpixels/(frame/s), which is slightly higher than the one in reference [16] (2.03 mW/Mpixels/frame/s)). The power supplies of [16] were separated into 3.3V (analog) and 1.8V (digital), which lowered down the power consumption of digital circuitry significantly, finally lowered down the total power consumption of the system. The image sensor in reference [16] was implemented using 0.18 μm process technology, which had more than 50% saving on the power consumption comparing to 0.35μm process for a same circuit with same power supplies.

The proposed design used higher power supply (3.3V) for digital circuitry and was fabricated using 0.35μm technology. So those issues highlighted above could be the reasons of higher power consumption in proposed work. If we assume that the resolution of ADC, power supply and technology are the same for both works, a sample image (Lena 512×512) is taken into simulation based on the operating methodologies of both designs. The comparison table in Figure 4.26 shows that the total conversion steps saved is around 23.17% and total switching energy saved is 17.65% for the proposed work comparing to

Architecture	SAR[3]	This work
Supply voltage	3.3V/1.8V	3.3V
Power consumption (mW/Mpixels .frame/s)	2.03	2.115
Resolution of ADC	14 bits	9 bits
Main design requirement	12-bit cap array	Prediction scheme
Technology	0.18µm 2P3M	0.35µm 2P4M
Pixel resolution	4112x2168	98x98
Frame Rate (Frame/s)	60	2082
Power consumption	0.145 mW	0.1175 mW

Parameters	SAR[3]	This work	Saved
Conversion steps	2.1M	1.6M	23.17%
Switching Energy	711J	585.5J	17.65%

Suppose same ADC resolution and same unit capacitance and Vref.

Figure 4.26: Comparison table with another work [16] with sample image Lena.

the reference one. Therefore, this proposed design does decrease the power consumption of the CMOS image system through the prediction scheme based on the architecture of SAR ADCs.

4.5 Remarks

The simulation pictures are stored in a dropbox file, the link to view all the original pictures is:

https://www.dropbox.com/sh/zobxuzspgqlh9jf/AADsduv8JsiMjqrClay6wJxua?dl=0 which is free access.

Chapter 5

Design Improvement:A New ADC Prediction Scheme

Based on the operation principle of the proposed prediction scheme in Chapter 4, shown in Figure 5.1, a checking step is utilized after A/D conversion of LSB to keep the algorithm more robust. The correctness of the predicted MSBs is determined after an A/D conversion cycle. Two A/D conversion cycles are utilized for an analog input, if the predicted MSBs are estimated incorrect. The A/D conversion steps of an analog input with correct predicted MSBs are reduced, but the steps using incorrect predicted MBSs are increased. Finally, the total A/D conversion steps saved using the prediction scheme is not optimized, as well as the switching energy saved, although the saving on both aspects are significant reduced according to Matlab simulation results shown in Figure 4.15. Therefore, an improved prediction scheme using a new method of correctness checking is described in this chapter to optimize the savings on total conversion steps and switching energy.

5.1 New Prediction Checking Methodology

The operation principle of the improved prediction scheme is illustrated in Figure 5.2, where the new prediction checking is implemented. When the predicted MSBs are predicted, the prediction checking is utilized to determine their correctness before an A/D

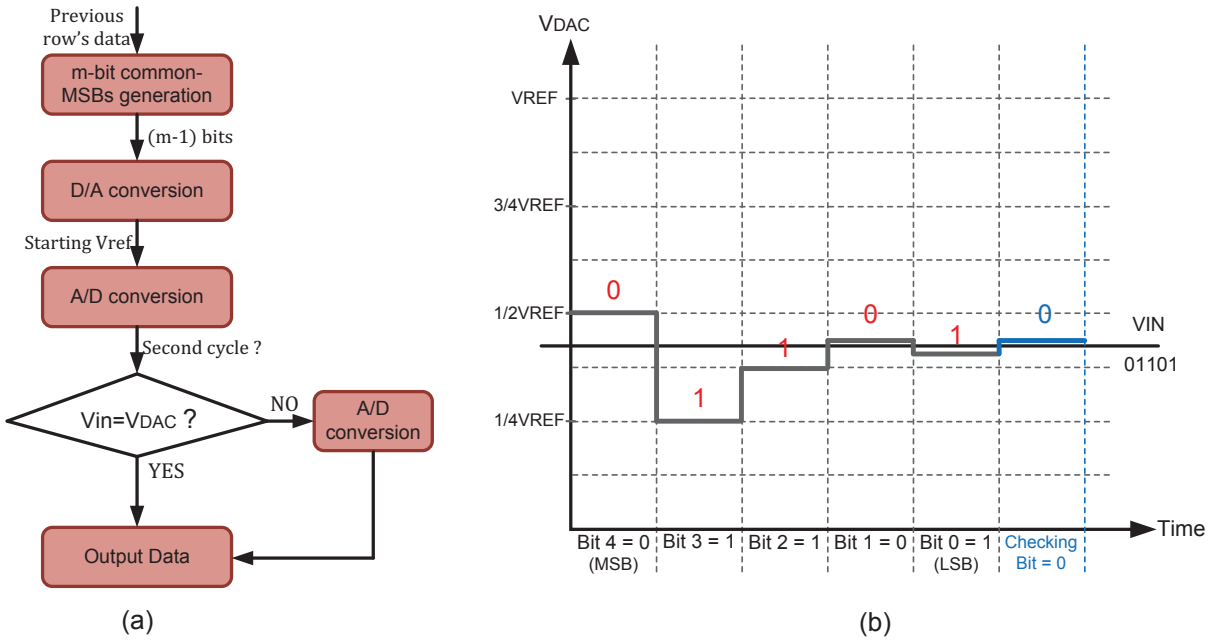


Figure 5.1: The prediction scheme: (a)Operation principle, (b)A/D conversion diagram of a 5-bit ADC.

conversion cycle. If the predicted MSBs are predicted correctly, the corresponding analog value V_{start} using D/A conversion is utilized in A/D conversion steps for the left bits. Otherwise, the predicted MSBs are discarded and the final quantization values are obtained by a complete A/D conversion cycle. Finally, the correct digital code of the analog input is reported as an output of the ADC system. One A/D conversion cycle is utilized in the improved prediction scheme if the prediction is incorrect, which improves the sampling frequency of the SAR ADCs and minimizes the total conversion steps of a frame.

The A/D conversion steps of two analog inputs with two predicted MSBs using a 5-bit SAR ADC are illustrated in Figure 5.3, where the prediction for both inputs are estimated correctly. The step sizes of an A/D conversion cycle in a 5-bit ADC are summarized as follow: $\frac{1}{2}V_{REF}$, $\frac{1}{4}V_{REF}$, $\frac{1}{8}V_{REF}$, $\frac{1}{16}V_{REF}$, $\frac{1}{32}V_{REF}$. The size of each conversion step is half of previous step based on the binary searching algorithm. The moving direction of each

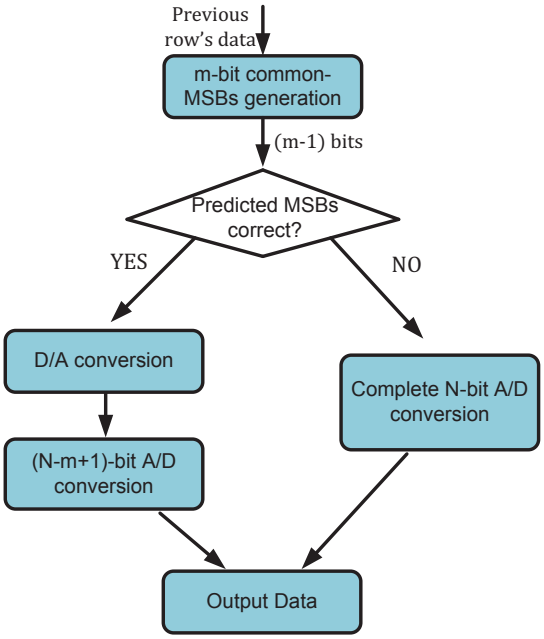


Figure 5.2: Operation principle of the improved prediction scheme.

conversions step is determined by the previous quantized value. Up movement is utilized if previous quantized value is 1, otherwise down movement is utilized.

Using the analog input shown in Figure 5.3(a) for example, its corresponding digital code is 01101 and the predicted MSBs are 01 with two bits (means m=2). The starting reference voltage (V_p) $\frac{1}{4}V_{REF}$ (01000), and the allowable voltage range for A/D conversion of left bits is also $\frac{1}{4}V_{REF}$ (which is equivalent to $\frac{1}{2^m}V_{REF}$, where m=2). The moving direction of third conversion step (which is first step for A/D quantization) is upward, as its previous quantized value is pre-defined by the predicted MSBs. The voltage range of this analog input using A/D conversion steps is from $\frac{1}{4}V_{REF}$ to $\frac{1}{2}V_{REF}$. Using another analog input shown in Figure 5.3(b), its corresponding digital code is 00110 and the predicted MSBs are 00 with two bits (means m=2). The starting reference voltage (V_p) is 0V (00000), and the allowable voltage range for the left bits is $\frac{1}{4}V_{REF}$. It is the same as the example in Figure 5.3(a), but varies from 0 to $\frac{1}{4}V_{REF}$ as downward movement of third conversion step.

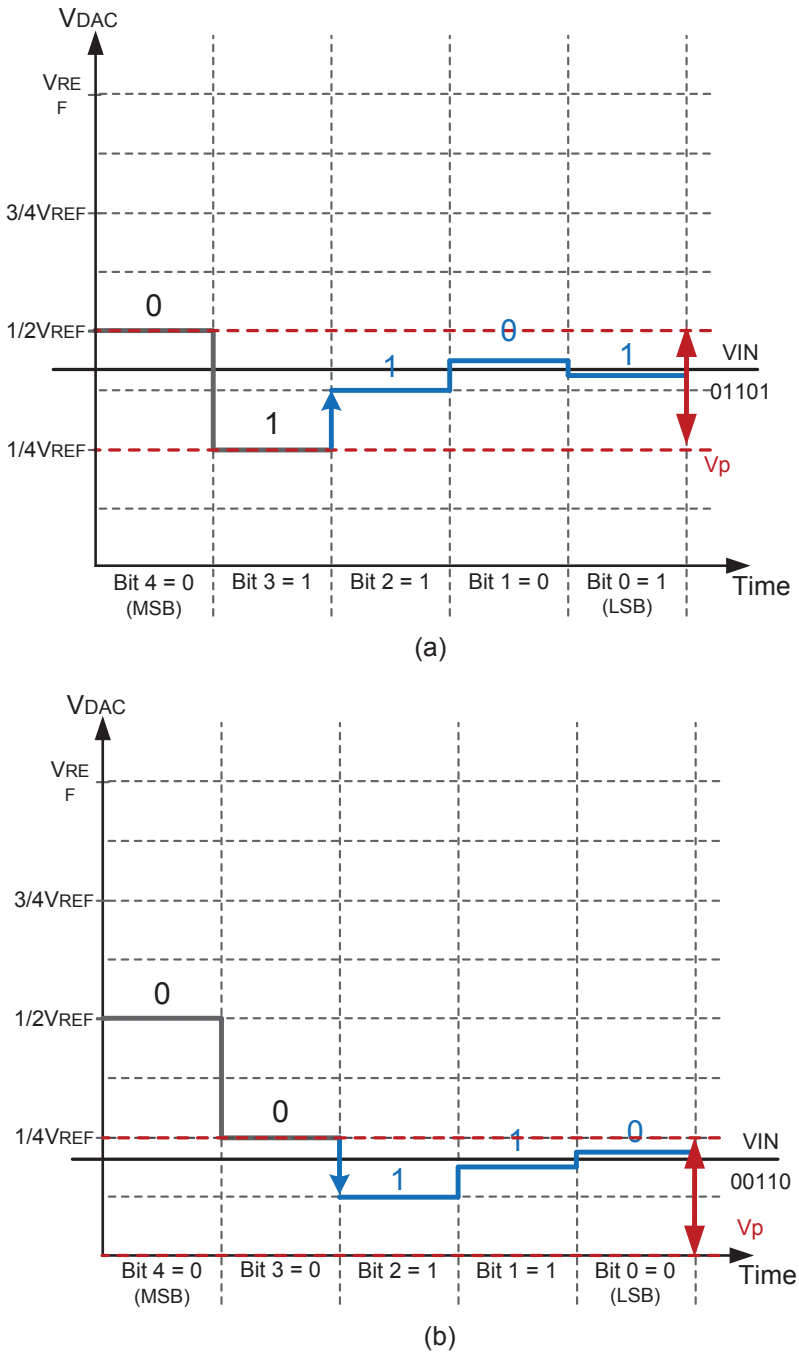


Figure 5.3: A/D conversion diagrams of two analog inputs: (a) 01101 with predicted MSBs 01XXX; (b)00110 with predicted MSBs 00XXX.

According to the analysis of the two examples shown in Figure 5.3, the necessary conditions of correct prediction are summarized in Eq. 5.1 and Eq. 5.2 with known predicted MSBs and an unknown analog input.

(i)

$$V_{in} - V_p < \frac{1}{4}V_{ref} = \frac{1}{2^m}V_{ref}$$
$$V_{in} < \frac{1}{2^m}V_{ref} + V_p \qquad \text{(Eq. 5.1)}$$

(ii)

$$V_{in} > V_p \qquad \text{(Eq. 5.2)}$$

where m is the number of predicted MSBs, $V_p = \frac{1}{4}V_{REF}$ in example (a) and $V_p = 0V$ in example (b). The two voltages consist of a voltage window to determine the correctness of the prediction using the predicted MSBs..

5.2 Simulation Results

Based on the operation principle of improved prediction scheme using the new prediction described in Figure 5.2, only one A/D conversion cycle is utilized for an analog input with incorrect prediction. The total A/D conversion steps implemented in both original and improved prediction schemes are summarized as follow:

(i) Correct Prediction:

No. of A/D conversion = N-m; for original prediction scheme;

No. of A/D conversion = N-m; for improved prediction scheme.

(ii) Incorrect Prediction:

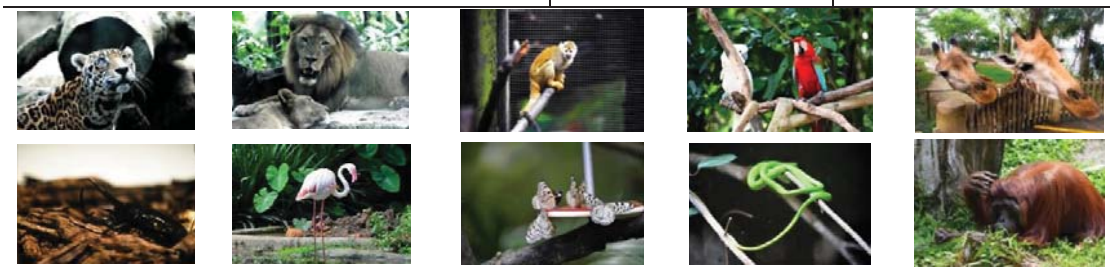
No. of A/D conversion = N + (N-m); for original prediction scheme.

No. of A/D conversion = N; for improved prediction scheme.

where N is the resolution of ADC and m is the number of predicted MSBs. If the prediction is estimated correctly, the numbers of A/D conversion are (N-m) for original and improved prediction schemes. Otherwise, the total conversion steps using original prediction scheme is (N-m) steps more than the steps using improved prediction scheme. The switching energy using improved prediction scheme is also significant reduced by reducing (N-m) A/D conversion steps compared with original one, when the prediction is estimated incorrectly. The same groups of images shown in Figure 4.15 in Chapter 4 are utilized for Matlab simulation, and the corresponding total conversion steps and switching energy using both original and improved prediction schemes are simulated. The simulation results are summarized in Figure 5.4, where the total conversion steps and switching energy are reduced significantly by both prediction schemes compared with the operating methodology of conventional ADCs. Around 4% to 5% of total conversion steps and switching energy are reduced by the improved prediction scheme compared with original one, which is contributed by reducing the (N-m) conversion steps of incorrect prediction using the original prediction scheme. m, the number of predicted MSBs, is frame dependent variable (varying from 1 to 8). N is the resolution of the ADC system, which is reported as 9 using the implemented image sensor. The amount of pixels with correct predicted MSBs is much larger than the one with incorrect predicted MSBs for most natural scenes. The amount of the conversion steps reduced by the improved prediction scheme is also frame dependent variable, which is relative small number compared with the total conversion steps. Therefore, the improved prediction scheme reduces the total conversion steps and switching energy in small amount (around 4% to 5%), and optimizes the sampling frequency of ADCs as well.

Standard Test Image (http://www.imageprocessingplace.com/root_files_V3/image_databases.htm)

Averaged Conversion steps Saved	21.44% (old)	**26.21% (new)**
Averaged Switching Power Saved	21.02% (old)	**25.59% (new)**

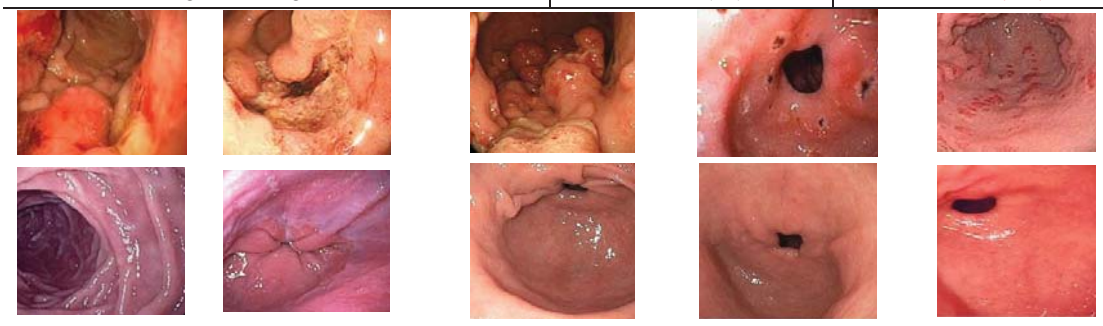


Images taken at Singapore Zoo

Averaged Conversion steps Saved	25.66% (old)	**30.73% (new)**
Averaged Switching Power Saved	29.07% (old)	**33.46% (new)**

Images taken at Venice, Italy

Averaged Conversion steps Saved	27.74% (old)	**33.23% (new)**
Averaged Switching Power Saved	31.16% (old)	**35.87% (new)**



Inner views of stomach and intestine.

Averaged Conversion steps Saved	31.04% (old)	**34.88% (new)**
Averaged Switching Power Saved	32.50% (old)	**35.58% (new)**

Figure 5.4: Total conversion steps and switching energy saved compare to the conventional SAR using improved prediction scheme for four groups of pictures.

5.3 Hardware Implementation

The architecture of a SAR ADC utilized with the improved prediction scheme is illustrated in Figure 5.5. The correct-estimation detector is moved in front of the SAR control logic, as the prediction checking is operated before a SAR A/D conversion cycle. The architecture of the 9-bit DAC and other circuit blocks remain the same as those implemented in the CMOS image sensor described in Chapter 4. The necessary conditions utilized for the new prediction checking are summarized in Eq. 5.1 and Eq. 5.2. The DAC implemented in the SAR ADC are reused to obtain the analog values of V_p and $(V_p + \frac{1}{2^m}V_{ref})$, and the comparator is utilized for two comparisons between the analog input and V_p or $(V_p + \frac{1}{2^m}V_{ref})$.

The operation principle of two comparisons (Eq. 5.1 and Eq. 5.2) using the 9-bit DAC and comparator is illustrated in Figure 5.6, where an analog input with the predicted MSBs (101XXXXXX) is used as an example. Initially, all capacitors in the DAC are initialized by connecting both top and bottom plates to lower reference voltage (V_{low}). In the next step, the first three capacitors remian connected to V_{high},V_{low},V_{high} respectively and others are connected to V_{low}, for the purpose of obtaining analog value of the prediction MSBs. The V_p shown in Eq. 5.1 is reported as output voltage of the DAC (V_{dac}) which is equivalent to 101000000, and the C_1 is reported as the comparison result between the analog input and V_p . Lastly, the last seven capacitors are connected to V_{high} and the first three capacitors remain the same connecting. The $(V_p + \frac{1}{2^3}V_{ref}$, where m =3)shown in Eq. 5.2 is reported as the output voltage of the DAC which is equivalent to 101111111, and the the C_2 is reported as the comparison result between the analog input and $(V_p + \frac{1}{2^3}V_{ref})$. The values of C_1 and C_2 are essential to define the correctness of the predicted MSBs. If they are estimated correctly, the values of C_1 and C_2 are summarized as follow:

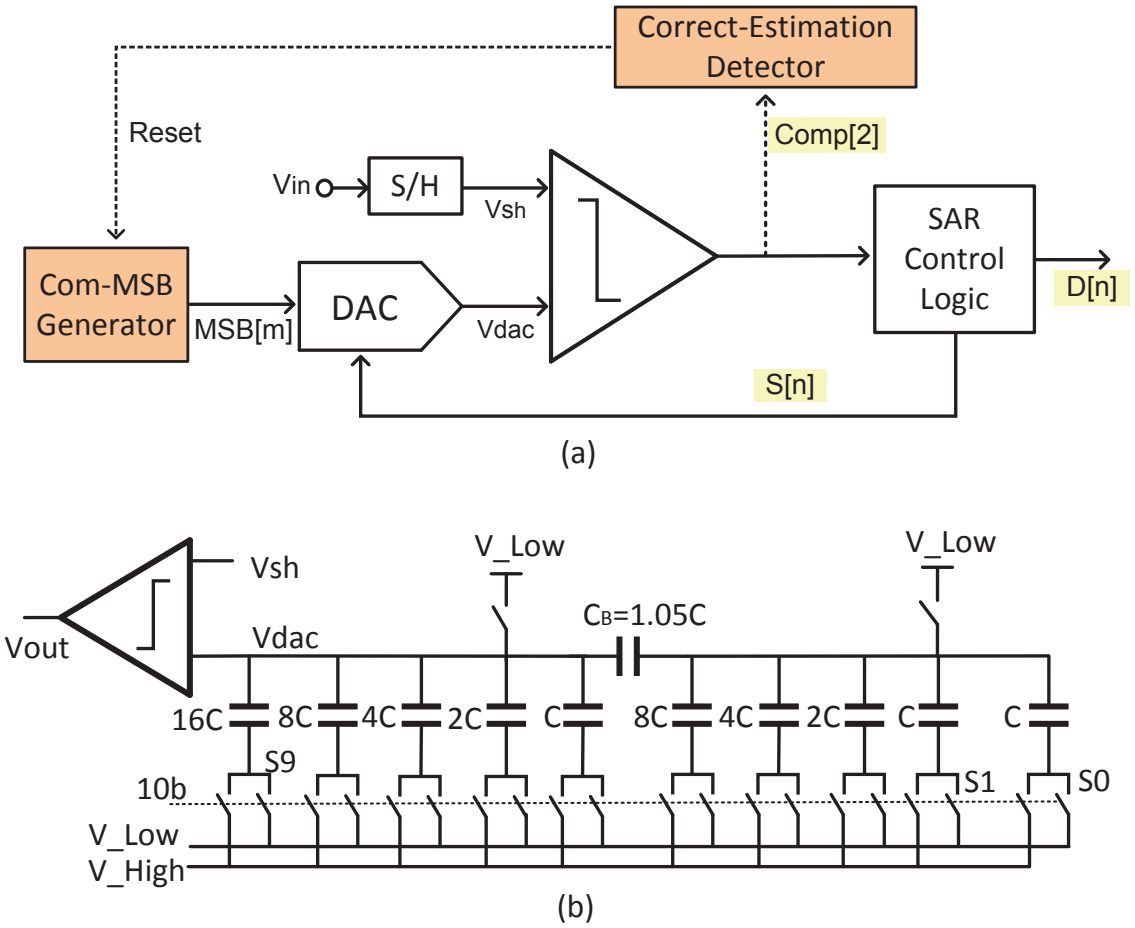


Figure 5.5: Updated architecture for SAR ADCs.

(i) $C_1 = 1 \Longleftarrow V_{in} > V_p$;

(ii) $C_2 = 0 \Longleftarrow V_{in} - V_p < \frac{1}{2^m} V_{REF}$.

The new prediction checking utilized in the SAR ADC system makes use of the DAC and comparator for the purpose of minimizing the complexity of the SAR ADC system.

In conclusion, the methodology of new prediction checking is innovated from the binary searching algorithm. The new prediction checking is implemented before an A/D conversion compared with the original algorithm, and the analog input is compared with a voltage window defined by the predicted MSBs. If the input voltage falls into the voltage window, the prediction is correct and the A/D conversion continues the quantization for left bits. Otherwise, the prediction is incorrect and a complete A/D conversion cycle is utilized with discarding the predicted MSBs. Compared with the original prediction scheme, only one A/D conversion cycle is implemented for an analog input using the improved prediction scheme with incorrect predicted MSBs. Both savings of the total conversion steps and switching energy are optimized and improved based on Matlab simulation using the improved algorithm, and it is significant to a CMOS image sensor for low-power application.

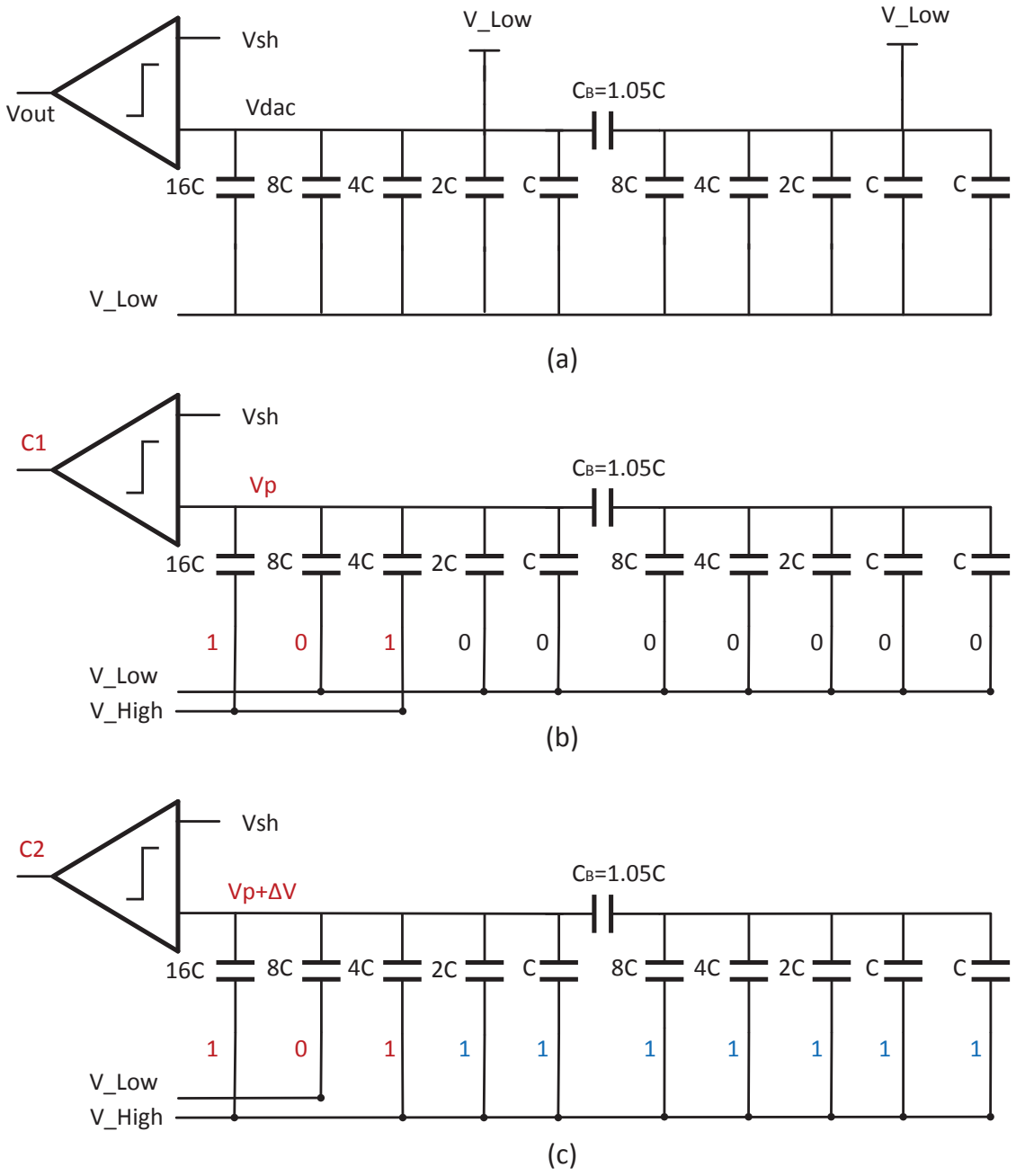


Figure 5.6: Operation principle of the new prediction checking.

Chapter 6

Conclusions and Future Work

6.1 Conclusion

This thesis demonstrates the research framework for the design of a CMOS image sensor with the proposed algorithm. Analysis of spatial likelihood in natural scenes in row by row scans performed by image sensors reveals, a strong correlation between the consecutive rows of most natural images is realized. This was the initial inspiration behind the idea of using previous-row data to predict pixels‘ few most significant bits (MSBs). The aim of the algorithm finally proposed was to reduce the number of A/D conversion steps needed for those MSBs and, by extension, the conversion energy consumed.

The first work investigated the basic framework of the algorithm for exploiting spatial likelihood in images. A prediction scheme was then proposed based on the known quantization results of previous-row pixels. Assuming that similar neighbor pixels in the previous row are the same as the selected pixel, then the common MSBs of those neighbor pixels should also be applicable to the selected pixel. So the predicted MSBs are initiated from it, and its value is one bit less of common MSBs. The bit numbers of the predicted MSBs are frame dependent variables, which vary for each selected pixel.

Since the predicted MSBs are obtained before the A/D conversion, there is no need for A/D conversion steps for those bits, thus reducing the energy required for conversion. In the SAR ADC system implemented for this design, the capacitive DAC was component

which consumed the most power. In the DAC system, the capacitor switching energy accounts for most of the total consumption and is proportional to the capacitance value. As the capacitors assigned for MSB operation are higher weighted, the reduced number of A/D conversion steps needed for the MSBs can make a significant contribution to the total saving in switching energy. Furthermore, several groups of natural images were included in a MATLAB simulation to compare the total A/D conversion steps and the total SAR ADC switching energy used in the proposed prediction scheme with those used in conventional A/D conversion methodology. The simulation results showed that a 20%-30% saving in total A/D conversion and switching energy are obtained using SAR ADC system operating methodology with this prediction scheme.

A prototype CMOS image sensor implemented with the proposed column-parallel SAR ADC system was fabricated using a 0.35μ m AMS process. The size of the sensor was 1.8mm $\times$ 3.5mm, with a 98 $\times$ 98 pixel array. The performance of this image sensor was tested and summarized. Comparison with a conventional SAR ADC for CMOS image sensors shows saving of around 23.17% in total conversion steps and 17.65% in total switching energy when the proposed prediction scheme is used.

Secondly, improvements were proposed in the operating methodology for the prediction scheme was proposed. Since a prediction correctness-checking step is performed at the end of the A/D conversion, a worst case total of 19 clock cycles are needed for a 9-bit ADC. This decreases the sampling frequency of the ADC, and the saving in A/D conversion steps is not maximized. Correctness checking for the predicted MSBs before A/D conversion was therefore proposed. In this prediction scheme, the maximum allowable movement for the left LSBs is bounded by a voltage range which can be estimated from the value and bit number of the predicted MSBs. The two boundaries of the voltage range can be used to determine the correctness of the prediction scheme: it is correct when the analog input is bounded inside; otherwise, it is uncorrect. The MATLAB sim-

ulation with the updated algorithm showed a 4% to 5% improvement in both total A/D conversion steps and total DAC switching energy.

6.2 Future Research Work

This prediction scheme proposed for the first time in this research project, was implemented for a number of natural scenes with high level of similarity. The number of reference pixels used in the prediction scheme and the bit numbers of the predicted MSBs used in this algorithm are defined by the user and by the properties of each frame, respectively. If different applications are used or the properties of the captured frames, the number of reference pixels used to predict MSBs can be changed to any number, and the bit numbers of predicted MBSs can be fixed or limited by a value. This can optimize the performance in different applications.

One possible avenue of future research would be to explore the use of this prediction scheme in endoscopy or capsule endoscopy, because, according ro the MATLAB simulation mentioned Chapter 4, the inner views of the stomach or intestine have very high levels of similarity. Actually, the degree of image resolution required for endoscopy is not as high as that needed for images of natural scenes, so the predicted MSBs could be directly applied as the quantization value of the selected pixels. If the image quality is acceptable, the bit numbers of the predicted MSBs can be fixed and directly assigned as digital output using this method, and the A/D conversion steps for the left LSBs can be disregarded. This modification to the proposed algorithm will result in a higher saving in A/D conversion steps and switching energy, and also speed up the A/D conversion cycles for pixel outputs. Future research might also focus on algorithm optimization, with particular regard to reference pixels, predicted MSBs and the operating methodology of column-level ADC systems.

Publication

Conference Papers

(i) **Lifen Liu**, Hang Yu and Shounshun Chen, "Low-Power Column-Parallel ADC for CMOS Image Sensor by Leveraging Spatial Likelihood in Natural Scene," in *IEEE Sensor Conference*, pp. 1196-1199, Valencia Spain, Nov. 2014.

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