

A novel low power Pulse Width Modulation vision sensor with handshaking read-out strategy

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Abstract--A novel vision sensor based on pulse width modulation scheme and asynchronous communication protocol is presented. The pixel includes only 20 transistors and occupies an area of $18.5 \times 18.5 \mu\text{m}^2$, with a fill factor of 23% using $0.35 \mu\text{m}$ CMOS process.

I. INTRODUCTION

Real time image acquisition and processing is becoming a challenging task because of higher spatial and coding resolution, which imposes very high bandwidth requirement. In order to alleviate some of these problems, address event representation [1] combined with the spiking pixel architecture was proposed [2]. Despite the very promising concept of efficient allocation of the transmission channel to only active pixels, the proposed technique suffers from the inherent disadvantage of the spiking nature of the pixel which constantly fires and frequently requests access to the bus. This imposes higher constraints on the AER processing speed and induces more dynamic power consumption. In our paper we propose a new pixel in which information is coded in the width of the pulse (PWM) instead of the firing frequency. This allows us to save dynamic power consumption and to extensively reduce inefficiencies due to frequent requests of the bus.

II. VISION SENSOR BASED ON PULSE WIDTH MODULATION

A. Pixel description

The proposed pixel is shown in figure 1. It is composed of a reverse biased photodiode P_d with internal capacitance C_d , transistor $m1$ for global reset and $m2$ for asynchronous self-reset, transistors $m3$ - $m7$ for event generation and $m15$ - $m17$ for latching the asynchronous self-reset signal. The rest transistors are responsible for realizing the communication handshaking with both the row and the column AER circuits.

An active low pulse \overline{Rst} is used to reset the pixels after which the integration process starts. Once the photodiode reaches the threshold voltage of the inverter, a request signal is sent to the row AER. Once this request is acknowledged, the pixel will send again a request to the column AER and once the later is acknowledged the pixel is reset by turning on transistor $m2$. The pixel remains at this stand-by state until a new frame capture cycle begins.

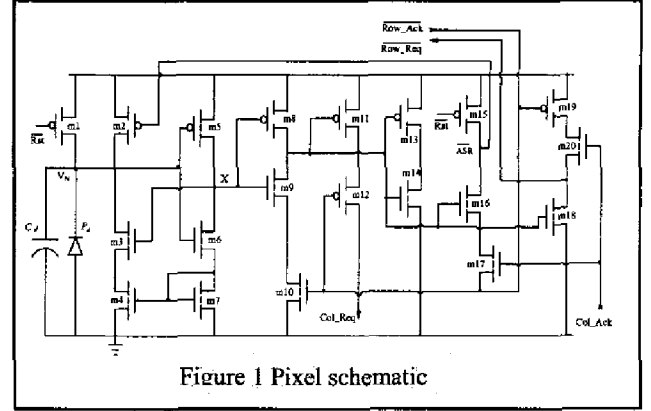


Figure 1 Pixel schematic

Figure 2 shows the simulation results of our pixel. The signals shown from top to bottom correspond to the photodiode voltage, the row request, the row acknowledgement, the column request, and the column acknowledgement, respectively.

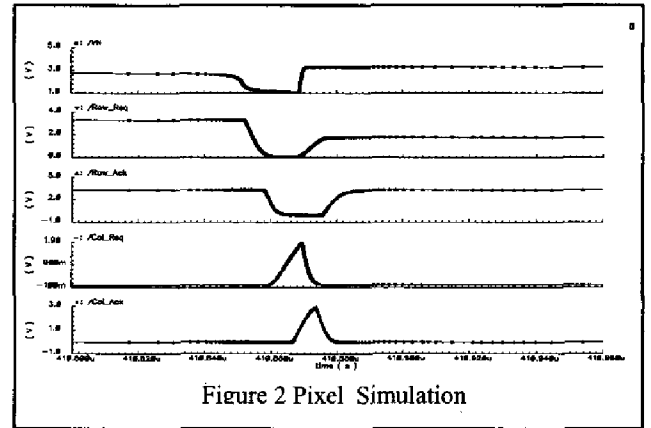


Figure 2 Pixel Simulation

B. Imager Architecture

The architecture of our imager is shown in figure 3. It includes the pixels array, row and column AER, row and column address encoder, timing controller and buffers between both the column and the row AER and the pixels array. When one or more pixels within a row fires this row will send a request " $\overline{Row_Req}$ " to the Row AER. The Row AER may receive several requests at the same time. After arbitration, only one row will be acknowledged. The fired pixels within the acknowledged row then send request " $\overline{Col_Req}$ " to the column AER. Instead of waiting for

the Column AER to acknowledge the requests one by one, the Column Buffer will hold their requests and acknowledge back concurrently. This improves the processing speed of Column AER by avoiding charging and discharging the large capacitance associated with the column buses. The column AER just needs to process the requests held by the column buffers. The combination of Row and Column acknowledgements will uniquely locate a fired pixel. This pixel will kill the previous "Row_Req" which enables the Row AER to start another round of arbitration and thus a pipeline Row and Column AER processing is obtained.

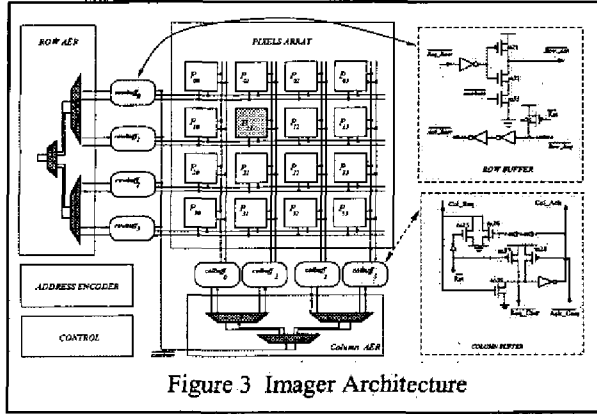


Figure 3 Imager Architecture

III. AER ARCHITECTURE

One of the major problems facing AER based imagers is the well known collision problem. At a given time the arbiter will grant access to the bus to only one pixel and will place the remaining fired pixels in a processing queue. A timing error is therefore induced which is proportional to the processing time of each request in the arbitration tree as well as the number of requests received at any given time.

A. Two-input fair arbiter

It is evident that a fair processing of the waiting queue helps to reduce the mean error. A fair 2-input arbiter is shown in figure 4 which could be divided into 3 units: arbitration unit, propagation unit and acknowledgement unit. The arbitration unit is constituted of an RS latch composed of two cross-coupled NOR2 gates and 5 additional transistors to switch the pulling down capability of the two NOR2 gates which is always toggled after arbitration has taken place. One should also note that the two NOR2 gates always have different pulling down capability and this allows avoiding meta-state of the RS latch.

B. Higher radix arbiter

To reduce the mean time error another solution is to reduce the processing time of the arbiter tree by building higher radix arbiters which could process more than two requests at the same time. The depth of the AER tree is reduced while the delay of one arbiter is kept at acceptable level, thus a faster

processing speed could be achieved. The 4-input arbitration unit is shown in figure 5. Four cross-coupled NOR4 gates are organized into *group0* and *group1*. Within each group, the principle of priority switch is the same as the one in the 2-input building block while a group priority signal "Groupswitch" is used to switch the priority between *group0* and *group1*.

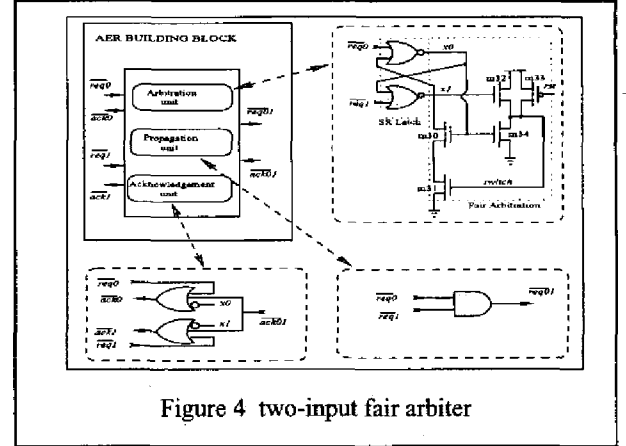


Figure 4 two-input fair arbiter

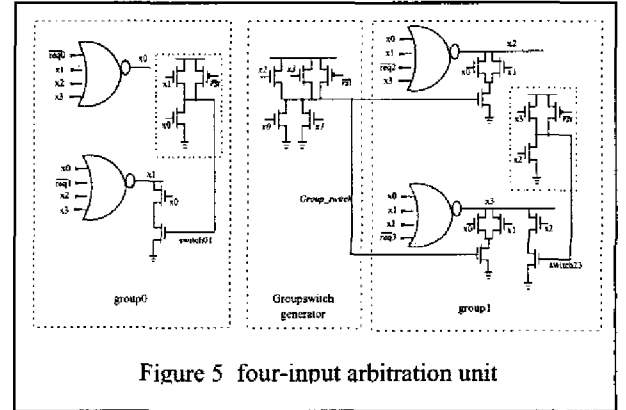


Figure 5 four-input arbitration unit

IV. CONCLUSION

A new pixel in which information is coded in the width of the pulse is proposed. The average current consumption of one pixel is 10nA, which is 3 orders of magnitude lower compared with that of the spiking pixel [3]. Transmission bandwidth and timing error due to collision are greatly improved. We also proposed a very simple and yet a reliable way to implement a fair arbitration which could be extended to higher radix architecture.

REFERENCE

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