On-Chip RF Energy Harvesting Circuit for Image Sensor

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***Abstract*— An on-chip RF energy harvesting circuit is integrated into an image sensor. The RF energy harvesting circuit is designed to function at 900 MHz. A DC voltage of 1.8V is achievable from the energy harvesting circuit output with -3 dBm input RF power. By charging up a 2.2 mF capacitor to 1.867 V, it has been demonstrated that the low-power image sensor functions well with the ability to obtain more than 1 frame of the image.**

Keywords- Image sensor, RF energy harvesting, RFID, autonomous sensor, Charge pump.

I. INTRODUCTION

Autonomous sensing and monitoring platform is an autonomous device that incorporating sensor, micro-controller, signal processor, power management circuitry, and wireless transceiver, etc [1]. This kind of sensing technology has gained increasing interests because it can be deployed without considering the wiring for power and signal transfer. It has promising applications such as Wireless Sensor Network and Structural Health Monitoring [2][3][4].

Battery remains to be a major limiting factor for the developing of truly autonomous deploy-and-forget sensing platform. If the sensing system could be powered by harvesting energy wirelessly from a low-power transmitter, it can almost require no attention once deployed. Prototypes of wirelessly powered sensing platforms for different applications have been reported in [1][6].

In this paper, a prototype of 64 by 64 pixels temporal difference image sensor with on-chip RF energy harvesting circuit is presented. The paper will be organized as follows. The design process and considerations for the RF energy harvesting circuit will be briefly described in Section II. Section III presents the measured I-V curve and the input impedance of the AC-DC voltage multiplier. The characterization result of the whole image sensor will be discussed in Section IV and finally Section V concludes this paper.

II. RF ENERGY HARVESTING CIRCUIT

The design of the far-field wireless RF energy harvesting circuit is illustrated in Fig. 1. The RF power received by the off-chip antenna is rectified and the DC power is stored in a storage capacitor. A matching circuit is designed for maximum power transfer between antenna output and rectifier circuit input. A voltage regulator is employed to provide stable DC voltage for the image sensor circuitry.

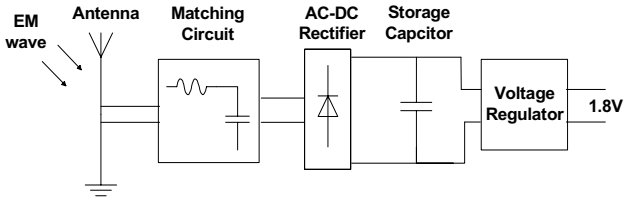


Fig. 1 Block diagram of RF energy harvetsing system

Due to the relatively large power consumption of the image sensor comparing to that of RFID (a few mini-watt vs. micro-watts), the image sensor must be designed to operate in the sleep-active cycle in order to function properly when integrated with the RF energy harvesting module. The image sensor remains in sleep mode until the voltage at the storage capacitor reaches a specific DC voltage. When the DC voltage reaches the required value, the image sensor wakes up and takes a snap of a scene. The image is then processed and stored. When the DC voltage drops below the required operating voltage level, the image sensor goes into the sleep mode again.

III. AC-DC VOLTAGE RECTIFIER

A multi-stage diode-capacitor voltage rectifier is adopted. The circuit is fabricated using UMC 0.18 μm CMOS process with the diode implemented using the diode-connected PMOS transistor. The schematic of the circuit is shown in Fig. 2. The circuit is not only capable of rectifying the AC voltage but also capable of boosting the output DC voltage to a higher level. The DC output voltage of this diode-capacitor rectifier can be expressed as follows:

$$V_{OUT} = 2N(V_{in} - \Delta V)\ ) \qquad (1)$$

Where Vin is the amplitude of the input voltage, N is the number of stages of the rectifier, and ΔV is the voltage drop across the PMOS transistor when the diode-connected transistor is turned on. Equation (1) shows that reducing ΔV will increase V_OUT. Thus a large W/L ratio is desirable but other factors like parasitic resistance, capacitance and leakage as well as the area occupied by the circuit needs to be considered during the design. A systematic analysis of designing the circuit on CMOS is presented in [7].

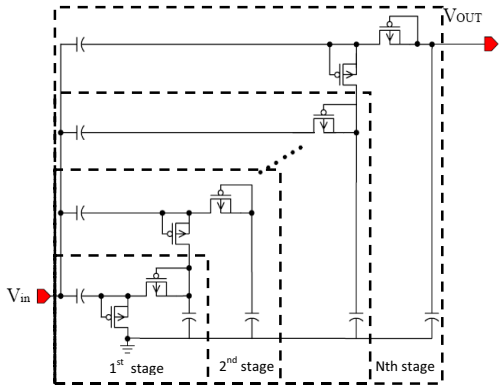


Fig. 2 PMOS implentation of AC-DC rectifier

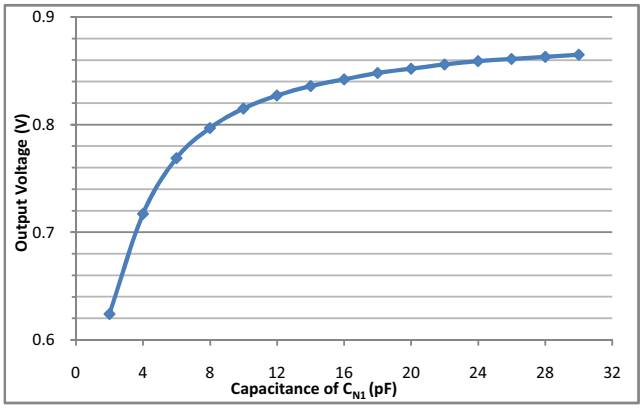


Fig. 3 Capacitor size versus output DC voltage of a single stage voltage rectifier. (note: the vertical axis represents the open-circuit DC voltage at the output)

Transistor with large W/L ratio leads to a significant leakage current when the transistor is reverse biased and it also introduces larger parasitic capacitance. The size of the transistor is chosen carefully by trading-off between the lower turn-on voltage and leakage. The body of PMOS is tied to the source to reduce the leakage current from the body.

The size of the capacitor for each stage also affects the performance of the whole circuit [7]. The capacitor cannot be too small otherwise so that the effect of the parasitic capacitance becomes significant and degrades the performance of the circuit. On the other hand, it cannot be too large due to area constraints. The value of the capacitor is chosen such that it is large enough to suppress the ripple at the output of each stage so that it can be nearly constant. To determine the optimal value of the capacitor, a simulation was carried out on a single stage rectifier. The input voltage is fixed at 0.6 V, the open-circuit DC voltage at the output was observed with varying value of the capacitor and the result is plotted in Fig. 3.

Fig. 3 shows that the output DC voltage increases with the size of the capacitor. But when the capacitor is larger than 10 pF, further increase in the capacitor value contributes little to further increase in output voltage. Thus the optimal capacitor size for our design was chosen to be 10 pF.

Once the sizes of transistor and capacitor are determined, the design of the each stage of the circuit is fixed. Multiple stages are stacked up in order to reach the required output DC voltage. More stages leads to a higher DC voltage with the input RF power kept constant. However, the increase in number of stages also increases the parasitic resistance and capacitance. These parasitic components degrade the Q factor of the input impedance and causes lower input voltage [8]. The number of stages is finalized to be six and the AC-DC voltage multiplier is integrated with the image sensor on the same die as shown in Fig. 4.

IV. OUTPUT CAHRACTERIZATION

Measurements are done to characterize the DC output with varying input received power. An RF signal generator at 900 MHz is used as a signal source and a source meter configured as current sink was connected at the output of the circuit as a load. The current drawn by the source meter is adjusted and the voltage across the source meter is measured. The input impedance at different input power can be measured with a Vector Network Analyzer. The power received at the input of the circuit is calculated based on the methodology presented in [9].

Fig. 5 shows the measured I-V curve. The various color zones represent different input power level in dBm. It can be seen that to charge up a capacitor to 1.8 V, a minimum input power of -3 dBm is needed.

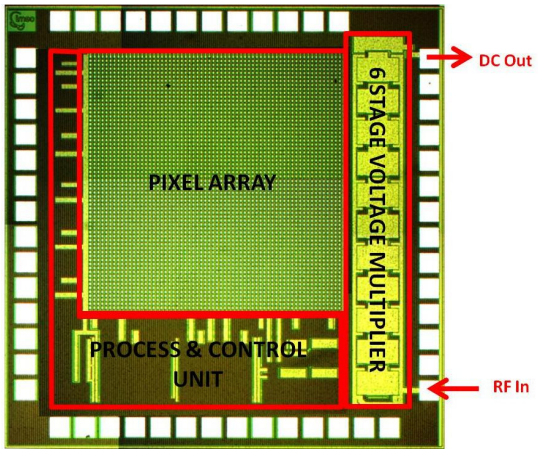


Fig. 4 IC photo of the image sensor with AC-DC rectifier

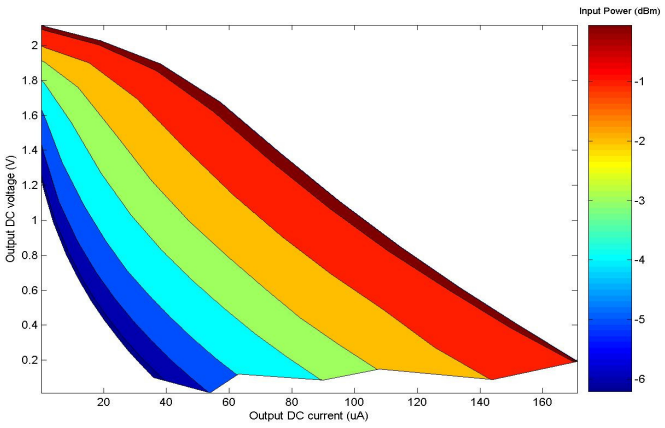


Fig. 5 Output DC I-V curve of the voltage mulitplier at 900 MHz.

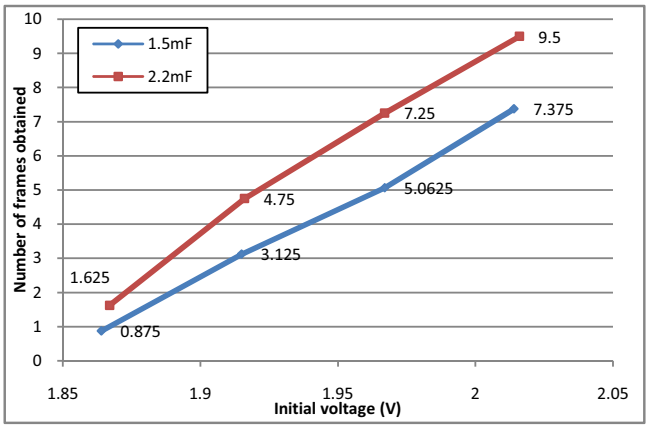
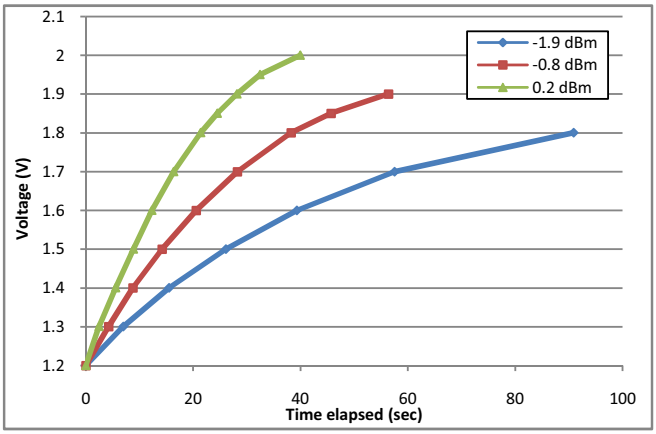
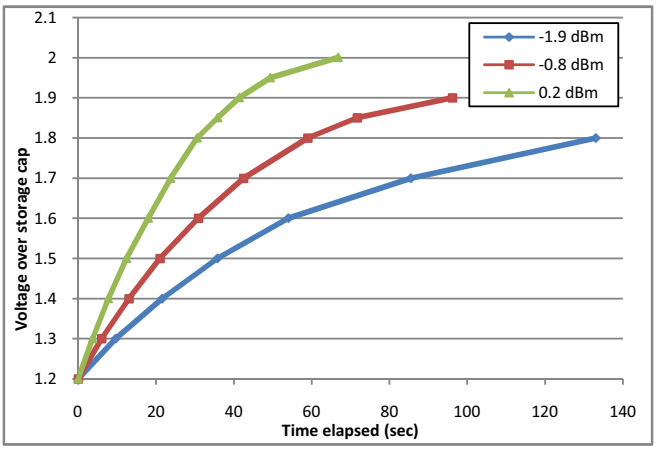


Fig. 6 No. of frames versus the initial voltage on the storage capacitor. (note: the value of the storage capacitor is 2.2mF)



(a)



(b)

Fig. 7 (a) Voltage over 2.2mF storage capacitor versus time elapsed. (b) Voltage over 1.5mF storage capacitor versus time elapsed. The legend shows the calculated input power.

V. MEASUREMENT RESULTS

The performance of the complete circuit is characterized with different input power, size of capacitor and amount of energy stored. Firstly, the storage capacitor is charged up to a certain voltage level and the image sensor is turned on. The energy stored in the capacitor will be consumed by the image sensor and the voltage across the storage capacitor decays. The number of frames captured by the image sensor during the process is recorded.

Fig. 6 presents the measured results. The horizontal axis represents the DC voltage over the storage capacitor right before the image sensor is turned on. The vertical axis shows the number of frames recorded. Since only one pixel is accessed at one clock cycle, and what has been recorded is actually the total number of pixels accessed during the process. No. of frames are obtained by divide the number by the resolution (64x64), which explains the reason why the number of frames being fractional.

As presented in Fig 6, either higher voltage or larger capacitor can provide more energy for the operation of the image sensor circuit as more energy being stored. The measurement result shown in Fig. 7(a) illustrates that it takes longer time to charge up larger capacitor to the same voltage level. Time was recorded from the instance when the voltage over the capacitor exceeds 1.2V until voltage over the capacitor stabilizes. The reason why 1.2V is chosen other than 0V is that the voltage over the capacitor will not drop to 0V during the operation as the circuits will cease to function when the supply voltage is below certain level. Throughout the measurement, the voltage is found out to be around 1.2V for the image sensor.

The maximum voltage over the capacitor is determined by the available input power and the performance of the RF-DC circuit. And the power consumption of the image sensor to obtain the required data determines the size of the capacitor. The above two factors together determines the charging time needed.

Although the RF signal generator serves as a good emulator as the terminal of the receiving antenna, still the device was attached to a receiving antenna to evaluate the performance of the prototype. The receiving antenna used was a planar monopole antenna fabricated on FR4 substrate. A log-periodic antenna was used as the transmitting antenna. The distance between the transmitter and the receiving antenna was set to be 1 meter due to the space constraint in the lab. The setup was surrounded by computers and equipment with people passing by from time to time. Thus the transmission-path loss is expected to be higher than that of the ideal free space.

Fig. 8 Image obtained by the 64x64 image sensor prototype

As a result, at the transmitting power of 29.5 dBm EIRP (23.4 dBm transmitting power and 6.1 dBi gain) the 2.2mF storage capacitor was charged up to 1.85V from 1.2V in 123 seconds and 1 frame of image was captured. As the maximum transmission power is capped at 36dBm EIRP, the maximum operating distance of the device is expected to be larger. Fig. 8 shows one of the sample image captured by the image sensor.

VI. CONCLUSION

A prototype of an autonomous image sensor powered by harvesting RF energy from a transmitter is presented. The energy harvesting circuit is integrated with the image sensor on the same die. The harvesting circuit operates at 900 MHz and a DC voltage of 1.8V is achievable with -3dBm input power. The performance of the sensor has been evaluated against the size of charge storage capacitor and the voltage over the storage capacitor. The circuit was attached to a receiving antenna and the measurement was done in the lab. The power from was 29.5 dBm EIRP (23.4 dBm transmitting power and 6.1 dBi transmitting antenna gain). With the receiving antenna 1 meter away from the transmitter, the circuit was able to charge the 2.2mF storage capacitor to 1.85V from 1.2V in 123 seconds and with this amount of energy, 1 frame of image was captured.

The performance of this prototype was limited by the internal leakage and the efficiency of the AC-DC voltage multiplier circuit. Further work is in progress to design the AC-DC voltage multiplier so as to optimize its conversion efficiency as well as reducing the leakage so that the required input power level can be reduced. A compact multi-antenna-multi-rectifier array will also be explored in order to capture more power so that the operating distance can be significantly increased for the next prototype.

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