Exploring the Novel Characteristics of Hetero-Material Gate Field-Effect Transistors (HMGFET's) with Gate-Material Engineering

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***Abstract*—The novel characteristics of a new type of MOSFET, the hetero-material gate field-effect transistor (HMGFET), are explored theoretically and compared with those of the compatible MOSFET. Two conceptual processes for realizing the HMG structure are proposed for integration into the existing silicon technology. The two-dimensional (2-D) numerical simulations reveal that the HMGFET demonstrates extended threshold voltage roll-off to much smaller length and shows simultaneous transconductance enhancement and suppression of short-channel effects (SCE's) [drain-induced barrier-lowering (DIBL) and channel-length modulation (CLM)] and, more importantly, these unique features could be controlled by engineering the material and length of the gate. This work demonstrates a new way of engineering ultrasmall transistors and provides the incentive and guide for experimental exploration.**

***Index Terms*—Asymmetric MOSFET, asymmetric spacer, channel-length modulation, drain-induced barrier-lowering, gate-material engineering, hetero-material gate FET.**

I. Introduction

As THE MOS ULSI technology is pushed into the deep-submicron era, two major questions arise. The first question is: How can the device performance for a given technology be improved? The second question is: How can the technology be scaled into smaller dimensions? Within the context of MOS device physics, the major limiting factors for MOSFET scaling are the so-called short-channel effects (SCE's), notably, threshold voltage (V_t) roll-off at decreasing gate length (L_g) as well as drain-induced barrier-lowering (DIBL) and channel-length modulation (CLM) at increasing drain voltage (V_{dd}). For logic applications, the major figures of merit are the drive current (on-state current, $I_{\rm on}$) and leakage current (off-state current, $I_{\rm off}$). For analog circuits, voltage gain is an important design parameter, given by the ratio of the transconductance over the drain conductance (g_m/g_d). The basic challenges in MOSFET scaling and reliability/performance optimization are the tradeoffs for V_t/V_{dd}, $I_{\rm on}/I_{\rm off}$, and g_m/g_d.

A conventional (i.e., symmetrical) MOS structure will eventually reach its scaling limit since, at very short gate length, the device operation is asymmetrical even at very small drain bias, resulting in DIBL and CLM. Unconventional MOSFET's employing asymmetric structures have been proposed [1]–[6] to overcome the bottleneck in transport efficiency and SCE's. The principal idea behind the asymmetric MOSFET is to tune the channel electric-field profile such that, compared to the symmetric MOSFET, it is larger at the source side to accelerate carriers and smaller at the drain side to reduce short-channel and hot-carrier effects. This can be achieved by asymmetric channel doping [1], asymmetric halo source (HS-GOLD) [2], asymmetric sidewall [3], asymmetric S/D implant [4], and dual-material gate (DMGFET) [5], [6]. Unlike asymmetric structures employing doping engineering [1]–[4] in which the channel field distribution is continuous, gate-material engineering with different workfunctions [5], [6] introduces a field discontinuity along the channel, resulting in simultaneous transport enhancement and SCE suppression. The idea is similar to what was achieved by applying different gate bias in dual-gate [7] or split-gate [8], [9] structures. However, the novel characteristics of the hetero-material gate field-effect transistor (HMGFET), as demonstrated experimentally [5] and predicted theoretically [6], promise to have significant impact if it can be realized in existing silicon ULSI technologies.

In this paper, the unique features of the HMGFET are explored and its performance in terms of V_t roll-off, DIBL, $I_{\rm on}/I_{\rm off}$, and g_m/g_d are compared with those of the conventional single-material gate MOSFET (SMGFET). The purpose of the work is to propose a new way of engineering deep-submicron MOSFET's with the focus on uncovering the potential benefits of the HMGFET in the context of a "compatible" process to realize the proposed HMGFET.

II. HMGFET Structure and Conceptual Processes

The key concept in the HMGFET is to introduce a step function in the potential along the channel such that the electric-field distribution is enhanced at the source side to increase the carrier velocity while the drain-potential change will be screened to reduce the SCE's [5], [6]. In the HMGFET structure, the gate consists of two materials in contact:

1) a poly-gate of length L_g and workfunction W_g defined by the technology feature length; and
2) a "source-gate" ("S-gate") of length L_s and workfunction W_s, where W_s should be chosen larger than W_g for an nMOS device [5].

The device has a channel length $L_c = L_g + L_s$ and its threshold voltage can be tuned by "engineering" the L_g/L_s ratio and the

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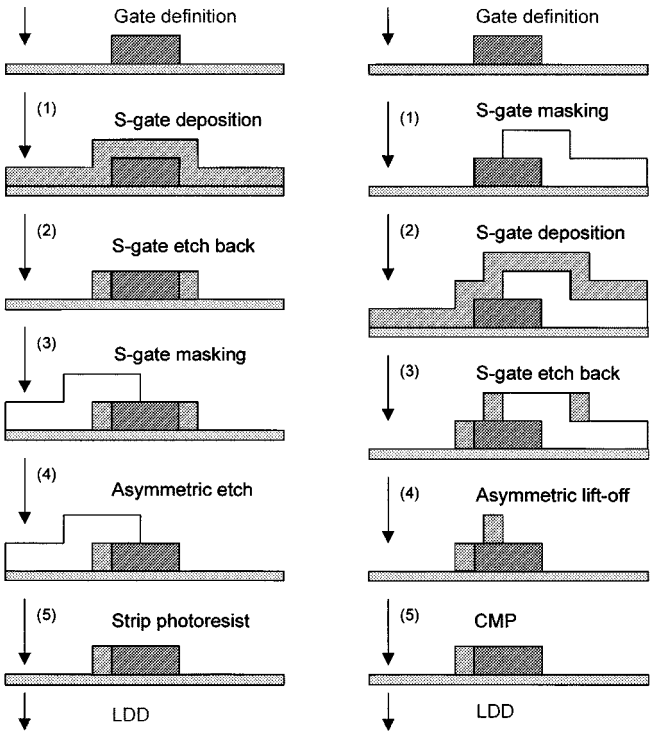


Fig. 1. Two conceptual processes to realize the proposed HMGFET with a length of L_s (S-gate spacer thickness), which require five additional steps inserted between gate definition and LDD formation of a conventional (SMG) process with gate length of L_g. The S-gate could be formed by either an asymmetric etch (left) or asymmetric lift-off (right) process.

workfunction difference $\Delta W_{sg} \equiv W_s - W_g$ for the location and the magnitude of the potential step at the hetero-material interface.

In order to realize the HMGFET in current MOS technology, it is assumed that the S-gate could be formed by a self-aligned asymmetric spacer process [6] with precise and uniform thickness control. Two conceptual processes are proposed, as illustrated in Fig. 1. Each process requires five additional steps inserted after gate definition and before LDD formation of a conventional (SMG) process. One additional mask is needed for the asymmetric S-gate, which requires a resolution better than the transistor gate length (L_g). It has been achieved for an 0.4-μm gate length within the error of 0.15 μm [3], and recently, for an 0.35-μm asymmetric LDD process using photolithography. The S-gate could be formed by either an asymmetric etch (Fig. 1, left) or asymmetric lift-off (Fig. 1, right) process (similar to [3]). Choices of the S-gate material and thickness are important design variables to be studied in the next section. The specific materials [10]–[12] and deposition/etching processes are left for experimental exploration.

III. Computer Experiments and Discussions

Four computer experiments are designed to explore the characteristics of the HMGFET with respect to those of a compatible SMGFET:

1) scaling characteristics with fixed L_s;
2) effect of L_g/L_s ratio at a fixed L_c;
3) effect of ΔW_{sg} at a fixed L_c;
4) performance comparison with SMGFET.

The major target parameters for comparison are as follows. The linear threshold voltage (V_{tlin}) is based on the maximum-g_m method (linear extrapolation of I_{ds}–V_{gs} to zero) at $V_{ds} =$ 0.05 V. The saturation threshold voltage (V_{tsat}) is based on a modified constant-current method at $V_{ds} = 3$ V where the critical current is defined as the drain current when $V_{gs} = V_{tlin}$ [13]. The saturation current ($I_{\rm on}$) is the drain current at $V_{gs} = V_{ds} = 3$ V. The leakage current ($I_{\rm off}$) is the drain current at $V_{gs} = 0$ and $V_{ds} = 3$ V (or $V_{ds} = 0.05$ V, as stated). The transconductance (g_m) is extracted from the slope of I_{ds} –V_{gs} at $V_{gs} = V_{ds} = 3$ V. The drain conductance (g_d) is extracted from the slope of I_{ds}–V_{ds} between $V_{ds} = 2$ and 3 V and $V_{gs} =$ 3 V. The major variables of investigation are: poly-Si gate length (L_g), S-gate length (L_s), S-gate workfunction (W_s), and channel doping (N_{ch}). N-channel device structures are created and simulated by the two–dimensional (2-D) device simulator MEDICI [14] to emulate an 0.25-μm CMOS technology [6] with $t_{ox} = 50$, Å $N_{ch} = 4 \times 10^{17}$cm^{-3}, $x_j = 70$ nm, and $W_g = 4.17$ eV. All device parameters for the HMGFET are equivalent to those for the SMGFET unless otherwise stated.

A. Scaling Characteristics with Fixed L_s

Transistor scaling characteristics (i.e., at reduced feature length, L_g) are studied for different (fixed) values of the S-gate length L_s, with all other parameters taking their nominal values. The workfunction of the HMGFET uses the default $W_g = 4.17$ eV for the polysilicon gate and $W_s = 4.63$ eV for the tungsten S-gate. The first, and probably the most significant, improvement over the SMGFET ($L_s = 0$) is the extended V_t roll-off down to much shorter length, as shown in Fig. 2. By adding a "spacer" of thickness $L_s =$ 70–80 nm to the source side of a conventional SMG process, V_{tlin} will not roll off until around $L_g = 0.08$ μm. Of course, it is not feasible to achieve the asymmetric spacer for the S-gate at $L_g = 0.08$ μm with lithographic means. However, this implies that, assuming the S-gate length (spacer thickness) L_s can be precisely controlled, threshold voltage will not be sensitive to L_g (poly-gate) variations at the 0.25-μm technology node, a desirable feature for deep-submicron technology. This is due to the fact that the S-gate of the HMGFET is the main control gate while the poly-gate serves as a screening gate [5]. Another unique feature of HMGFET is that V_t roll-off and roll-up can be controlled (tuned) by the S-gate length L_s, which is similar to the reverse short-channel effect (RSCE) commonly attributed to the boron pileup due to the S/D implant damage [15], but with a different mechanism. The V_t roll-off extension, or roll-up, is due to decreased L_g/L_s ratio (for fixed L_s) at decreasing L_g since the portion of the larger workfunction S-gate is increased as L_g decreases [6]. This feature will be fully investigated in Section III-B.

A second major improvement is the greatly reduced DIBL voltage ($V_{\rm DIBL} \equiv V_{tlin}$–$V_{tsat}$) as plotted against gate length [Fig. 3(a)] or channel length [Fig. 3(b)]. From a technology point of view, adding an S-gate spacer would reduce $V_{\rm DIBL}$ to below 0.1 V at $L_g = 0.2$ μm, as compared to 0.3 V for the SMGFET (of course, partially because of the added channel

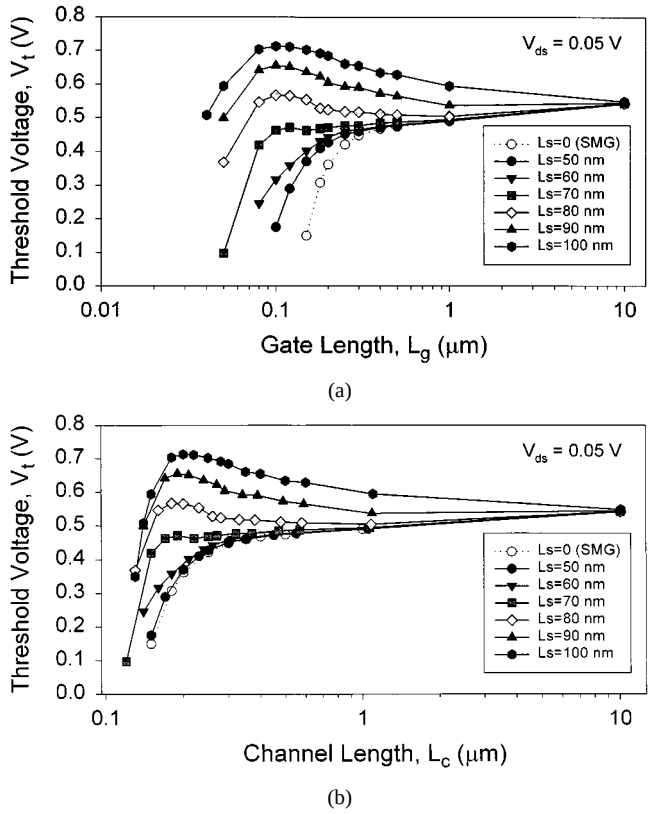


Fig. 2. Linear threshold voltage against (a) gate length or (b) channel length for different values of S-gate length, compared to the SMGFET (dotted line).

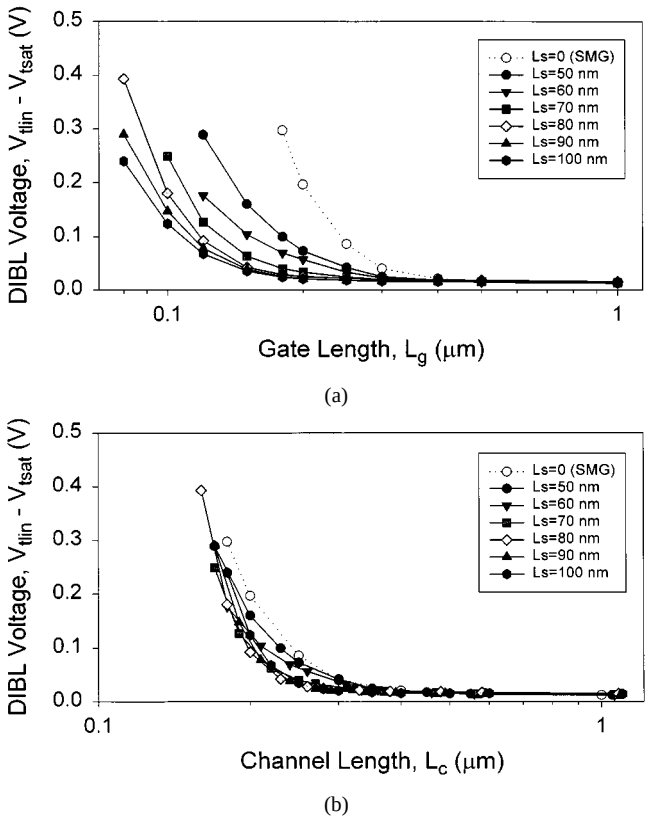


Fig. 3. DIBL voltage against (a) gate length or (b) channel length for different values of S-gate length, compared to the SMGFET (dotted line).

length for the HMGFET). From the device point of view, DIBL effect can be minimized with HMGFET compared to the SMGFET with the same channel length (at the expense of a smaller feature length L_g) (Fig. 4).

The $I_{\rm on}/I_{\rm off}$ tradeoff is also improved for the HMGFET, which shows a "flattened" region when $I_{\rm off}$ is plotted against $I_{\rm on}$ for the same devices with fixed L_s. This behavior is related to the extended V_t roll-off since $I_{\rm on}$ continues to increase as L_g reduces while $I_{\rm off}$ remains relatively unchanged before V_t rolls off.

B. Effect of L_g/L_s Ratio at a Fixed L_c

At a fixed channel length $L_c = L_g + L_s$, the location of the potential step can be tuned by different values of the L_g/L_s ratio. (The workfunctions for the poly/tungsten gates are still used.) This feature is investigated with L_s ranging from 0 (SMG) to 0.15 μm at a fixed $L_c = 0.25$ μm for the target parameters of V_{tlin}, V_{tsat}, $V_{\rm DIBL}$, $I_{\rm on}$, $I_{\rm off}$, g_m, g_d, and g_m/g_d, as shown in Fig. 5. It is observed that as L_s increases (L_g/L_s decreases), threshold voltage increases but there exists an optimum point where the DIBL voltage is minimum, which occurs when $L_s = 80$ nm (or $L_g/L_s = 2$, i.e., $L_g = 2L_s$ and $L_c = 3L_s$). This behavior (minimum $V_{\rm DIBL}$ for $L_g/L_s = 2$) has been consistently observed for other fixed values of L_c. This arises from the field redistribution as a result of the optimum location of the potential step (about one-third of the channel to the source side), which gives the most effective screening of the drain bias. This feature, combined with the insensitive V_t with L_g variation (Fig. 2), can be used to engineer

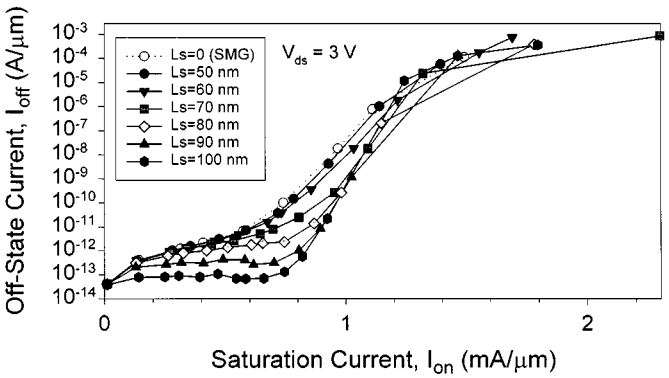


Fig. 4. Leakage current ($I_{\rm off}$) versus saturation current ($I_{\rm on}$) for different values of S-gate length, compared to the SMGFET (dotted line).

the HMG to minimize the DIBL effect. Further increase of L_s ($L_s \to L_c$, $L_g \to 0$) theoretically leads to an SMGFET with a larger workfunction (W_s).

However, as L_s increases (L_g/L_s decreases), saturation current decreases [Fig. 5(b)] although leakage current is also decreased. This is mainly due to the elevated threshold voltage at increasing L_s. On the other hand, simultaneous transconductance enhancement and drain conductance reduction has been achieved with HMGFET [Fig. 5(c)], which results in improved voltage gain. This is another unique feature of the HMGFET not easily achievable with doping engineering [1]. The reduced CLM effect in HMGFET is a result of the screening effect by the potential step, similar to DIBL reduction.

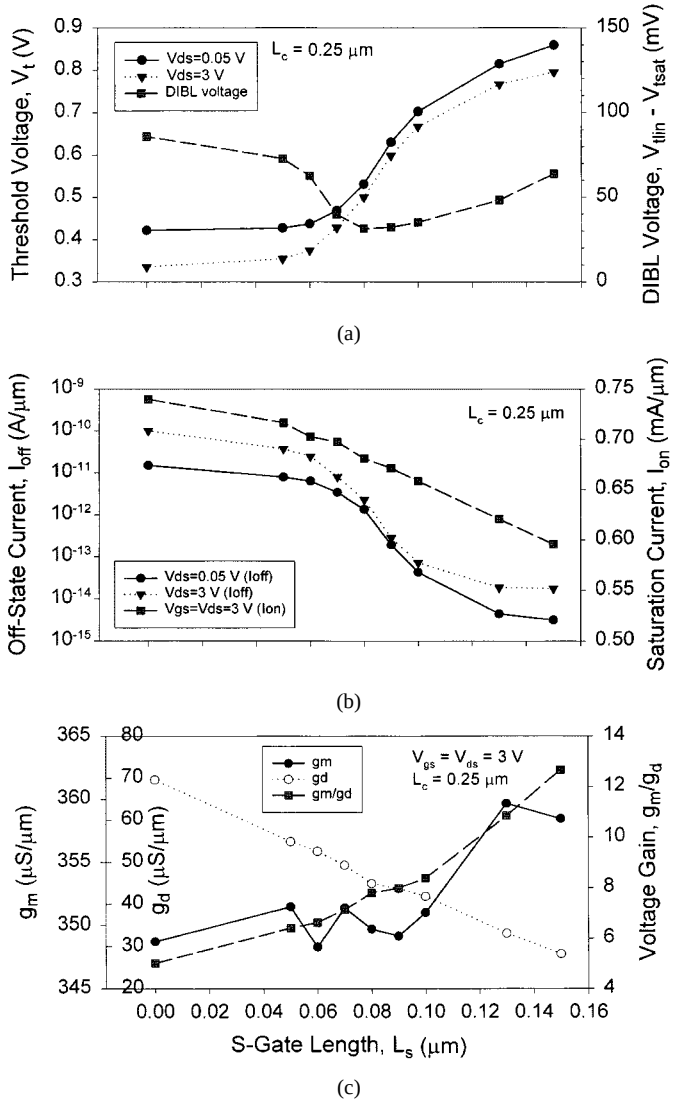


Fig. 5. (a) Linear and saturation threshold voltage and DIBL voltage, (b) saturation and leakage currents, and (c) transconductance, drain conductance, and voltage gain for different values of L_s at a fixed $L_c = 0.25$ μm.

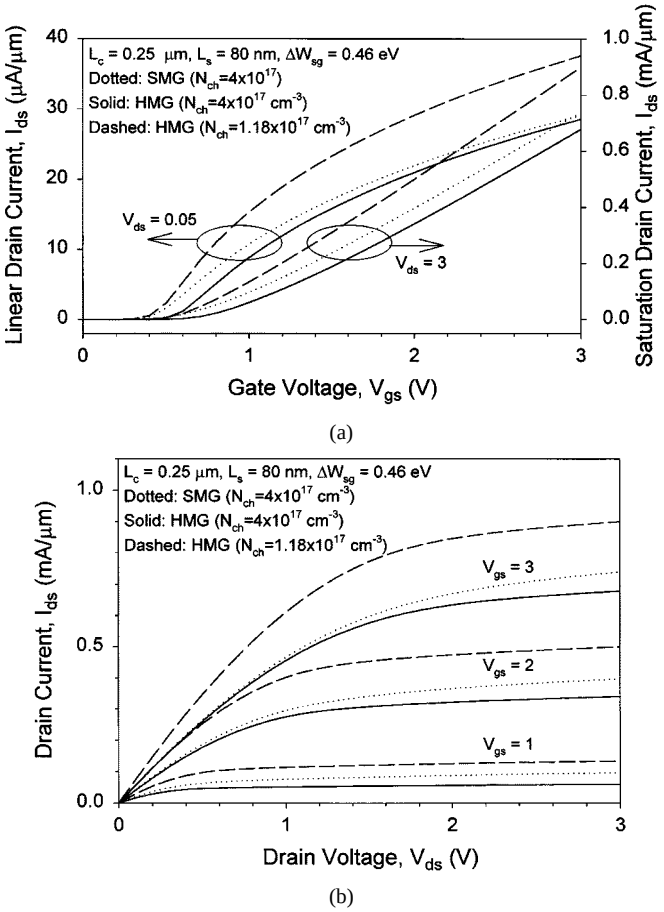


Fig. 6. (a) I_{ds}–V_{gs} and (b) I_{ds}–V_{ds} characteristics for the HMGFET's with $L_c = 0.25$ μm, $L_s = 80$ nm, and $N_{ch} = 4 \times 10^{17}$ cm^{-3} (solid lines) or $N_{ch} = 1.18 \times 10^{17}$ cm^{-3} (dashed lines), compared to the SMGFET with $L_c = 0.25$ μm and $N_{ch} = 4 \times 10^{17}$ cm^{-3} (dotted lines).

It appears from Fig. 5(a) that the optimum condition for DIBL reduction occurs in a region where V_t is most sensitive to L_s variation, which is very undesirable. As a matter of fact, this investigation is at fixed L_c (i.e., decreasing L_g with increasing L_s). Judging from Fig. 2(a) and assuming L_s is well controlled, $V_t - L_g$ is, in fact, much less sensitive to L_g variations in the optimum region ($L_g/L_s = 2$), which is a major feature of the HMGFET.

The I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics of a particular HMGFET with $L_s = 80$ nm and $L_c = 0.25$ μm ($L_g = 0.17$ μm) are shown in Fig. 6 (solid lines) and compared with the same SMGFET with $L_c = L_g = 0.25$ μm (dotted lines). g_m enhancement and g_d reduction are obvious from Fig. 6, but $I_{\rm on}$ is lower for the HMGFET. This is because V_t is larger for the HMGFET with the same channel doping ($N_{ch} = 4 \times 10^{17}$ cm^{-3}). However, the elevated V_t in HMGFET provides more room for V_t adjustment, such as reducing channel doping or gate oxide thickness, to boost the driving ability. When the HMGFET channel doping is reduced ($N_{ch} = 1.18 \times 10^{17}$ cm^{-3}) to obtain the same V_{tlin} = 0.422 V as that of the SMGFET, the HMGFET (dashed lines) shows a reduced g_d (22%) with improved g_m (50% and 17% in linear and saturation mode, respectively) and $I_{\rm on}$ (22%). This improvement, of course, is at the challenge of a much smaller gate length ($L_g = 0.17$ μm). However, on the other hand, the SMGFET will not work at this L_g. Complete performance comparison of the three devices is shown in Table I, in which the last column compares the HMGFET (with the same V_{tlin}) relative to the SMGFET. A similar experiment with $L_s = 70$ nm ($L_g = 0.18$ μm, $N_{ch} = 3.17 \times 10^{17}$ cm^{-3}) for the HMGFET has been carried out, and the results are shown in Table II.

C. Effect of Workfunction Difference at a Fixed L_c

In this experiment, the HMGFET with fixed $L_s = 80$ nm, $L_c = 0.25$ μm, $N_{ch} = 1.18 \times 10^{17}$ cm^{-3}, and $W_g = 4.2$ eV is taken to examine its performance parameters with varying S-gate workfunction values (from 4.2 to 5 eV). $W_g = 4.2$ eV, instead of 4.17 eV, is chosen for simplicity. The results are shown in Fig. 7 as a function of the workfunction difference ΔW_{sg}. The $\Delta W_{sg} = 0$ case corresponds to the SMGFET with the same $N_{ch} = 1.18 \times 10^{17}$ cm^{-3}. Like the L_g/L_s-ratio dependence, a minimum $V_{\rm DIBL}$ also occurs, which happens to be at $\Delta W_{sg} = 0.46$ eV (i.e., $W_s = 4.66$ eV). (Previous experiments

TABLE I
PERFORMANCE COMPARISON OF HMGFET ($L_s = 80$ nm, $L_c = 0.25$ μm) WITH SMGFET ($L_c = L_g = 0.25$ μm)

	SMG	HMG	HMG	
N_{ch} (cm^{-3})	4×10^{17}	4×10^{17}	1.18×10^{17}	–70.5%
V_{tlin} (V)	0.422	0.531	0.422	0
V_{DIBL} (mV)	86	31.4	40.5	–52.9%
I_{off} (A/μm)	1×10^{-10}	2.3×10^{-12}	1.17×10^{-10}	+17%
I_{on} (mA/μm)	0.74	0.681	0.9	+21.6%
g_m (μS/μm)	348.73	349.72	406.33	+16.5%
g_d (μS/μm)	69.63	44.93	54.29	–22%
g_m/g_d (V/V)	5	7.8	7.5	+50%
S_t (mV/dec)	88.63	89.34	90.09	+1.6%

TABLE II
PERFORMANCE COMPARISON OF HMGFET ($L_s = 70$ nm, $L_c = 0.25$ μm) WITH SMGFET ($L_c = L_g = 0.25$ μm)

	SMG	HMG	HMG	
N_{ch} (cm^{-3})	4×10^{17}	4×10^{17}	3.17×10^{17}	–20.8%
V_{tlin} (V)	0.422	0.468	0.422	0
V_{DIBL} (mV)	86	39.8	40.7	–52.7%
I_{off} (A/μm)	1×10^{-10}	7.96×10^{-12}	2.56×10^{-11}	–74.4%
I_{on} (mA/μm)	0.74	0.7	0.75	+1.4%
g_m (μS/μm)	348.73	351.38	366.11	+4.7%
g_d (μS/μm)	69.63	49.34	52.71	–24.3%
g_m/g_d (V/V)	5	4.1	7	+40%
S_t (mV/dec)	88.63	86.3	84.56	–4.6%

for the HMGFET's also had $\Delta W_{sg} = 4.63 - 4.17 = 0.46$ eV.) The significant result of this investigation is the tunability of threshold voltage by "gate-workfunction engineering" (0.5-V V_t adjustment with a variation of the workfunction difference of $\Delta W_{sg} = 0.8$ eV), which provides another degree of freedom (and supposed controllability) for transistor design.

On-/off-state currents also exhibit similar behavior as that of the L_g/L_s-ratio variation [Fig. 7(b)] as a result of increased V_t at increasing ΔW_{sg}. Increased ΔW_{sg} (i.e., larger potential step at the hetero-material interface) also favors g_m enhancement and g_d reduction and, thus, larger voltage gain [Fig. 7(c)].

To probe the physical mechanisms responsible for the improved performance of the HMGFET, surface electric-field and electron-velocity profiles across the channel for the three devices used in Fig. 6 are shown in Fig. 8. The two HMGFET's

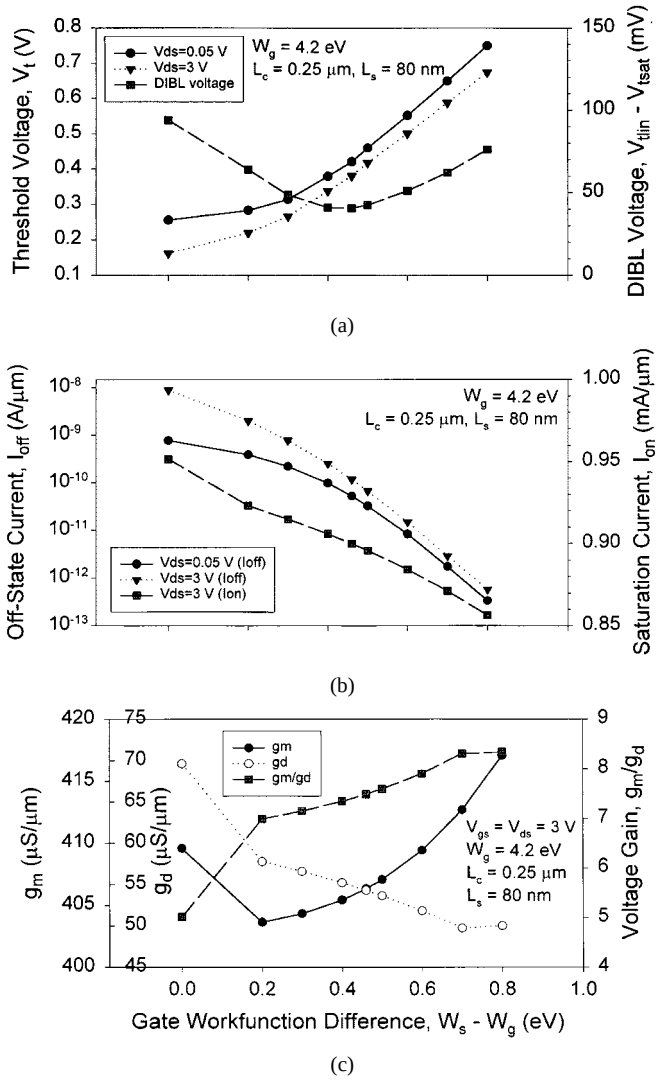
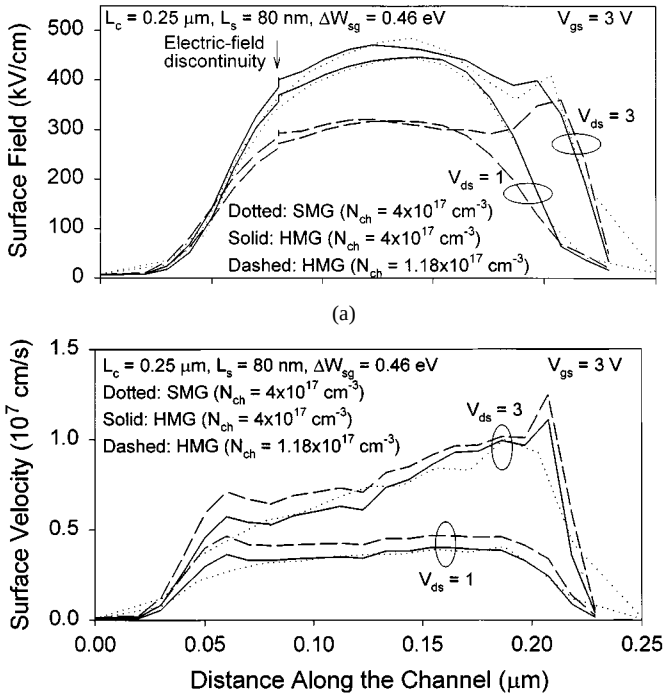


Fig. 7. (a) Linear and saturation threshold voltage and DIBL voltage, (b) saturation and leakage currents, and (c) transconductance, drain conductance, and voltage gain for different values of W_s at a fixed $W_g = 4.2$ eV for the HMGFET with $L_c = 0.25$ μm and $L_s = 80$ nm. The $\Delta W_{sg} = 0$ case corresponds to the SMGFET with the same $N_{ch} = 1.18 \times 10^{17}$ cm^{-3}.

are "optimized" in terms of minimum $V_{\rm DIBL}$, with $L_s = 80$ nm and $\Delta W_{sg} = 0.46$ eV. The electric-field discontinuity at one-third of the channel causes the overall channel field to be "flattened" (increased at the source side), resulting in larger average velocity when the electrons enter into the channel from the source. The potential step (field discontinuity) also forces channel field to redistribute mostly at the drain side as the drain bias is increased (from 1 to 3 V). This screening effect is responsible for the observed reduction in DIBL and CLM. The above behaviors are more pronounced for the HMGFET with a lower channel doping (dashed lines), in which transport efficiency is enhanced as a result of enhanced electron mobility and velocity in most of the channel region.

D. Performance Comparison with SMGFET

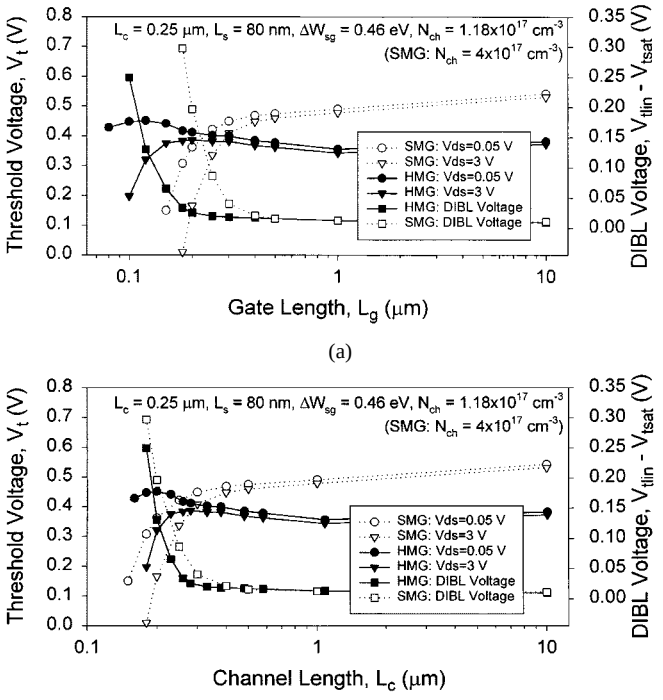
So far, the performance comparisons have been made between the HMGFET and SMGFET with the same L_c. One may argue that this is not a fair comparison, since the HMGFET re-



(a)

(b)

Fig. 8. (a) Electric field and (b) electron velocity along the surface of the channel for the three devices in Fig. 6. The two HMGFET's have $L_c = 0.25$ μm, $L_s = 80$ nm, $W_s = 4.66$ eV, $W_g = 4.2$ eV, and $N_{ch} = 4 \times 10^{17}$ (solid lines) or $N_{ch} = 1.18 \times 10^{17}$ cm^{-3} (dashed lines), compared to the SMGFET with $L_c = 0.25$ μm and $N_{ch} = 4 \times 10^{17}$ cm^{-3} (dotted lines).



(a)

(b)

Fig. 9. Linear and saturation threshold voltage and DIBL voltage against (a) gate length or (b) channel length for the HMGFET with a fixed $L_s = 80$ nm, $\Delta W_{sg} = 0.46$ eV, and $N_{ch} = 1.18 \times 10^{17}$ cm^{-3}, compared to the SMGFET ($N_{ch} = 4 \times 10^{17}$ cm^{-3}).

quires a much smaller feature length ($L_g = 0.17$ μm) and is more difficult to implement. Of course, if we used the HMGFET with $L_g = 0.25$ μm (so $L_c = 0.33$ μm), $I_{\rm on}$, $I_{\rm off}$, and $V_{\rm DIBL}$ would all be smaller; on the other hand, the SMGFET with $L_g = 0.17$ μm would not work since its V_t has already rolled off.

Now we compare the scaling characteristics (varying L_g) of the performance parameters of two transistors:

1) the "optimized" HMGFET (with fixed $L_s = 80$ nm, $W_s = 4.66$ eV, $W_g = 4.2$ eV, and $N_{ch} = 1.18 \times 10^{17}$ cm^{-3}); and
2) the conventional SMGFET ($N_{ch} = 4 \times 10^{17}$ cm^{-3}).

Both devices have the same $V_{tlin} = 0.422$ V at $L_c = 0.25$ μm. There are two scenarios for the comparison: for the same technology node (L_g), the HMG process is as if an asymmetric spacer is added to an existing SMG process; for device current–voltage (*I–V*) characteristics, however, the same channel length (L_c) should be compared. Results of this comparison are shown in Figs. 9–11.

It is observed that V_t roll-off can be compensated and tuned by the addition of the S-gate spacer. V_t roll-off has been extended down to much smaller L_g and, hence, V_t will be less sensitive to L_g variations [Fig. 9(a)]. The DIBL voltage can be greatly reduced at comparable technology (L_g) or device (L_c) [Fig. 9(b)]. Screening of the electric field effectively reduces the modulation of the effective channel length by the drain potential, resulting in much reduced drain conductance and, hence, increased voltage gain at small gate sizes, even with sacrifice in transconductance at the same technology node (L_g) (Fig. 10).

It is quite obvious that HMGFET can effectively reduce DIBL and CLM effects due to the screening of V_{ds}. The major disadvantage seems to be the lower drive current compared to the SMGFET with the same L_g, due to the added L_s. The ultimate performance comparison in terms of $I_{\rm on}$ versus $I_{\rm off}$ is made, as shown in Fig. 11. For the two devices with the same L_g, saturation ($I_{\rm on}$) and leakage ($I_{\rm off}$) currents (shown in the same symbol pair for each L_g) are plotted: a) as a ratio against L_g and b) in pairs. The extension of constant $I_{\rm on}/I_{\rm off}$ ratio down to much smaller L_g is a result of the extended V_t roll-off. The HMGFET exhibits a unique log($I_{\rm off}$) versus $I_{\rm on}$ behavior with an extended "flat" region, also due to the extended V_t roll-off. At the designed 0.25-μm technology node, the HMGFET can achieve comparable $I_{\rm on}$ and $I_{\rm off}$ to those of the SMGFET (triangles), even with the added S-gate spacer ($L_s = 80$ nm). Technology (L_g) could be further scaled (down to $L_g = 0.12$ μm with $I_{\rm off}$ < 0.2 nA/μm in this example) with HMGFET, at which time the SMGFET counterpart will no longer work.

From Fig. 9, one may have noticed that the improvement of the HMGFET is, in fact, a result of the V_t roll-up ("RSCE") which is absent from the SMGFET. However, this roll-up is due to a different mechanism than that of the normal RSCE, which results from the halo-implant damage and channel boron pileup and, thus, is not well controllable. Moreover, it is speculated that such RSCE may be reduced in an HMGFET structure because of the added S-gate spacer and, hence, the V_t roll-up could be well controlled by engineering the length and workfunction of the S-gate.

One natural question about the proposed HMG process would be whether it is feasible and worthwhile to explore

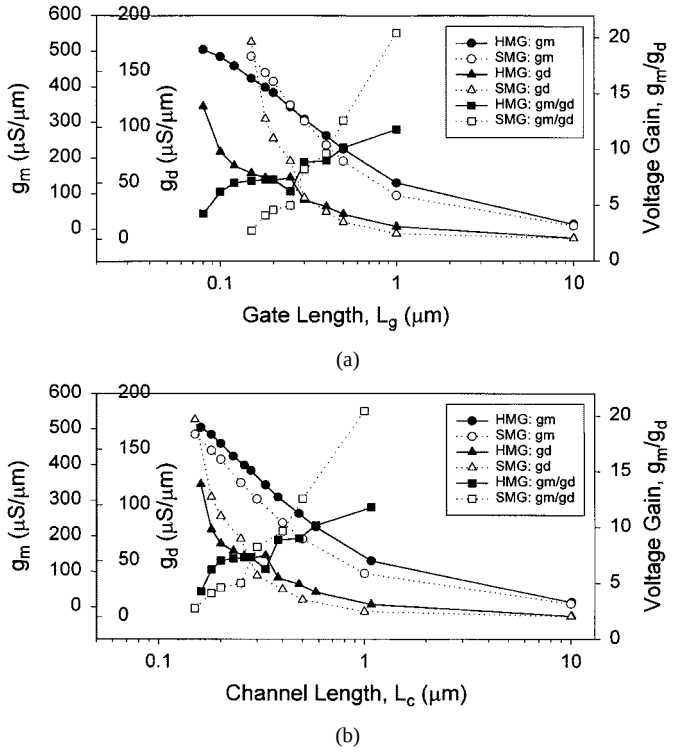


Fig. 10. Transconductance, drain conductance, and voltage gain against (a) gate length or (b) channel length for the same devices as in Fig. 9.

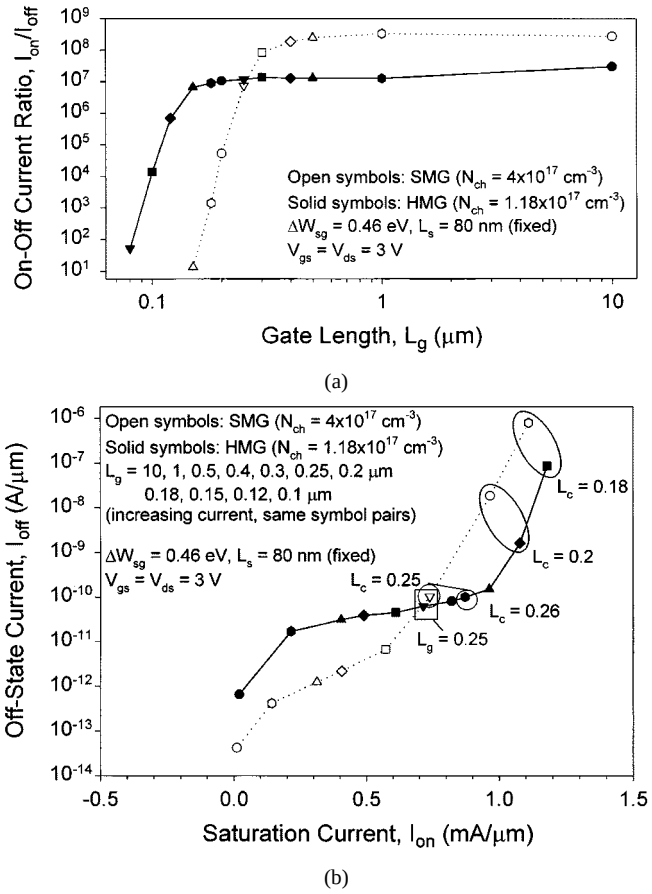


Fig. 11. For the same devices as in Fig. 9, saturation and leakage currents (shown in the same symbol pair for each L_g) are plotted: (a) as a ratio against gate length and (b) in pairs.

at the current technology node and beyond. This work has answered the two questions posed at the beginning of the paper. Device performance could be improved over a conventional SMG technology with the addition of the proposed HMG process, which should be feasible with photolithography in the sub-half-micron regime. Although not simulated, it is speculated that the predicted benefits of the HMGFET should still hold at sub-0.1-μm length. However, it will not be feasible with the existing lithographic means unless a new process is invented for the HMG technology. The most recent technology advancement [16] has demonstrated a 50-nm vertical MOSFET with lithography-independent gate length, which opens the door for realization of the proposed HMG technology. The controllable threshold voltage at affordable scaling (one of the grand challenges of the SIA's National Technology Roadmap for Semiconductors) the HMGFET could offer should promise to be attractive. With a properly "engineered" HMGFET, it is possible to further scale the device beyond what is achievable with conventional scaling rules.

Another complication for the HMGFET is the asymmetric MOS structure, which, if realized, may require a paradigm shift in the circuit design. However, asymmetric MOSFET's may be the ultimate solution for breaking the barrier of conventional MOS scaling limit. On the other hand, the proposed HMG process may also be employed in symmetric structures, i.e., adding a layer of material with different workfunction to both sides of the gate (like a LDD spacer). This would have an effect similiar to that of self-aligned tilted ion implantation [17] for controlling V_t roll-up, in which pockets of high-doping regions are created at the edge of the gate-controlled depletion region [18].

IV. Conclusions

The novel properties of a hetero-material gate transistor have been explored in the context of potential integration into the existing silicon ULSI technology. The unique features of the HMGFET, which are not easily achievable in conventional MOS technology, include: extension and controllability of threshold voltage roll-off and roll-up,minimum DIBL effect controlled by gate-material engineering (thickness and workfunction), simultaneous transconductance enhancement and SCE suppression. And most of all, these benefits could in principle be well controlled by a new way of engineering the ultrasmall transistors. This, of course, is based on the assumption that the S-gate length and workfunction could be well controlled by a "spacer" rather than "lithography" process.

Most criticisms on a theoretical prediction of a new phenomenon are the lack of experimental support. It is difficult to imagine having two gates side-by-side when making one gate is getting more and more difficult as the technology is driven to its limit. However, today's impossibility does not preclude tomorrow's reality. The significance of this investigation lies beyond the specific results obtained from the simulation. It is hoped that this work will inspire incentive for experimental exploration of the HMGFET, and will provide a guide to further research and experimental realization.

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