A Novel Approach to Compact *I- V* Modeling for Deep-Submicron MOSFET's Technology Development with Process Correlation

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The objective of this work is to develop a compact MOSFET model with minimum measurement data and model parameters as well as a one-iteration parameter extraction for deep-submicron MOS technology development. This has been achieved with our novel approach in model formulation, which results in a unified *one-region* equation that resembles the *same form* as the long-channel equation. It has been verified with experimental data from 0.25-µm CMOS shallow trench isolation (STI) technology wafers.

To summarize the unique features of our approach: (i) Accurate modeling of threshold voltage (V_t), based on the "$I_{crit}@V_{t0}$" definition [1] in which series resistance (R_{sd}) is embedded, is first carried out, which does not require any knowledge of mobility and series resistance but is a critical point on the I–V curve. The V_t model has 11 parameters including physically-derived nonuniform doping and workfunction (N_{ch}, $\boldsymbol{j}_m$), charge sharing ($\boldsymbol{l}$, $\boldsymbol{d}_0$), barrier lowering ($\boldsymbol{a}$, $\boldsymbol{j}_0$), V_t roll-up ($\boldsymbol{b}$, $\boldsymbol{k}_0$, $\boldsymbol{k}_1$), and DIBL ($\boldsymbol{d}_1$, $\boldsymbol{j}_1$). (ii) Effective channel length (L_{eff}) (or lateral LDD diffusion, $\boldsymbol{s}$) is determined together with V_t, with a fixed $\Delta L = 2\boldsymbol{s}x_j$. (iii) Semi-empirical mobility model ($\boldsymbol{m}_{eff0}$) has 3 (physical) parameters ($\boldsymbol{m}_1$, $\boldsymbol{m}_2$, $\boldsymbol{m}_3$) to be extracted from long-channel $I_{ds} - V_{gs}$ (low V_{ds}, zero V_{bs}) data, followed by bulk-charge factor ($\boldsymbol{z}$) extraction at high V_{ds}. At long channel, R_{sd} and channel-length modulation (CLM) are insignificant. (iv) With fixed L_{eff}, R_{sd} is modeled semi-empirically by $R_{ext} + \boldsymbol{u}'(V_{gs} - V_t)$, and extracted at short channel ($\boldsymbol{r}$; $\boldsymbol{u}$) where CLM can still be ignored at low V_{ds}. (v) With a newly-derived saturation voltage (V_{dsat}) and the extracted V_t, $\boldsymbol{m}_{eff0}$, and R_{sd}, CLM is modeled based on quasi-2D velocity overshoot [2] but has the same I_{ds} form with a new effective Early voltage (V_{Aeff}) to be fitted to the $I_{dsat} - L_{drawn}$ data (for $\boldsymbol{x}$). (vi) The on-state I_{ds} model ("1st-order") is then extended to subthreshold ("2nd-order") with an effective gate overdrive (V_{gteff}) replacing $V_{gs} - V_t$, which differs from BSIM formulation [3] with the correct diffusion current for all V_{ds} but still retains the same compact form. Only one parameter (V_{off}) is required to be extracted from the $\log(I_{ds}) - V_{gs}$ data with *minimum* V_t where edge-leakage current has minimum contribution. (vii) A novel approach to modeling edge-leakage current ("3rd-order") in STI structures demonstrates the accuracy and efficiency of our model. The same MOS $I_{ds}(L_{drawn}, W, V_t)$ equation is extended to model the edge-leakage current with a new width W_{e0} and a scaled threshold $\boldsymbol{V}_0 V_t$, together with a diode-leakage current (I_{s0}) added to I_{ds}, by fitting to the $\log(I_{ds}) - V_{gs}$ data with *maximum* V_t (@L_{drawn} = 0.8 µm) where edge leakage is most significant compared to the main MOS current. Following [4] for V_t process correlation, this paper presents prediction of on and off currents on other wafers with a simple diode-leakage correlation to implant dose from long-channel device.

Our model requires only 13 I–V sweeps (10 for extracting $I_{crit}@V_{t0}$) plus 42 point (I, V) measurements, with one-iteration 11 steps to extract its 23 parameters. The BSIM3v3 parameters are extracted with BSIMPro automatic extraction using <u>*all*</u> available I–V data. Sample results are shown (Figs. 1, 2), in which <u>*none*</u> of the I–V data has been used in our model extraction. Prediction of I_{on}/I_{off} for wafers #17~#19 (Figs. 3, 4) is also fully done by our model with implant dose ($\boldsymbol{F}$) as input without use of those wafer data.

The potential impact of our I_{ds} model as well as the *approach* is tremendous in providing a quick and reliable tool for deep-submicron technology developers and a circuit model with process variables as input.

[1] X. Zhou, K. Y. Lim, and D. Lim, *IEEE Trans. Electron Devices*, vol. 46, no. 4, p. 807–809, Apr. 1999.

[2] P. K. Ko, *VLSI Electronics: Microstructure Science*, vol. 18, 1988, p. 25.

[3] Y. Cheng *et al*., *BSIM3v3 Manual*, University of California, Berkeley, 1996.

[4] X. Zhou, K. Y. Lim, and D. Lim, to appear in *IEEE Trans. Electron Devices*, vol. 47, no. 1, Jan. 2000.

<u>Topic</u>: ***Process, Device and Circuit Simulation*** (<u>Special Session</u>: *Compact Modeling for Deep-Submicron Technology Development and Device/Circuit Design*)

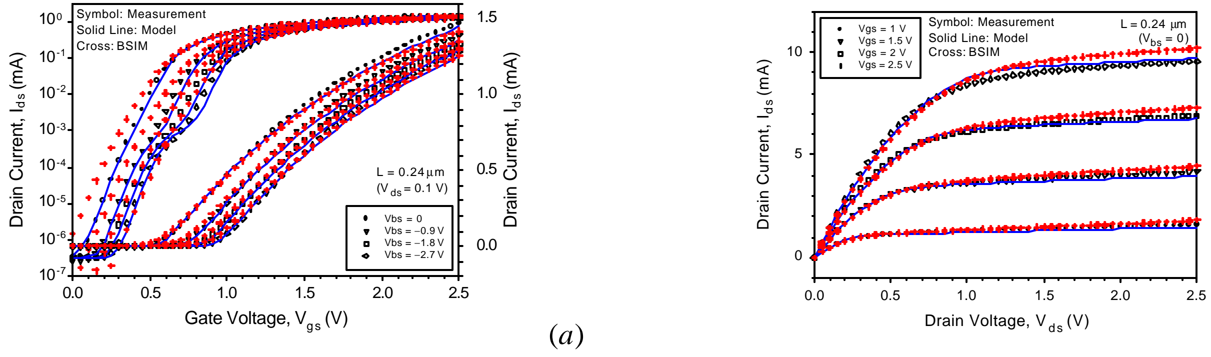

Fig. 1 (*a*) $I_{ds} - V_{gs}$ (*left*: log; *right*: linear) and (*b*) $I_{ds} - V_{ds}$ plots for the 0.24-μm device (*symbols*) compared to BSIM (*crosses*).

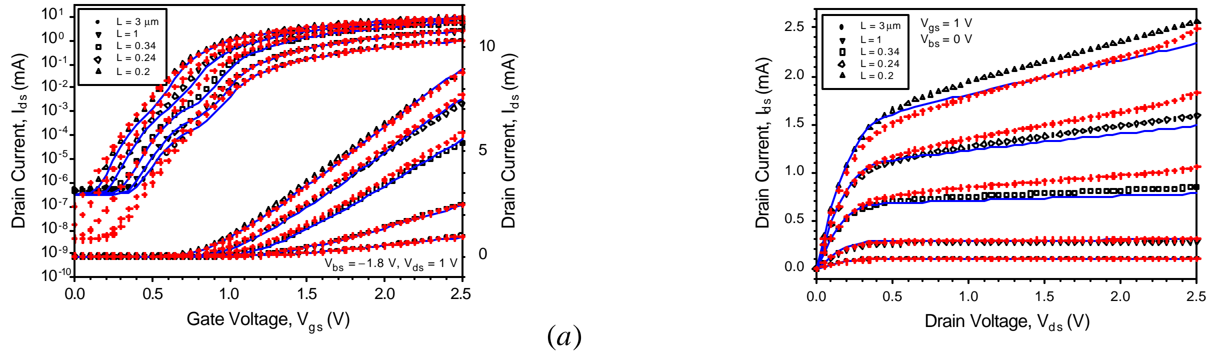

Fig. 2 (*a*) $I_{ds} - V_{gs}$ (*left*: log; *right*: linear) and (*b*) $I_{ds} - V_{ds}$ plots (*lines*) for five devices (*symbols*) compared to BSIM (*crosses*).

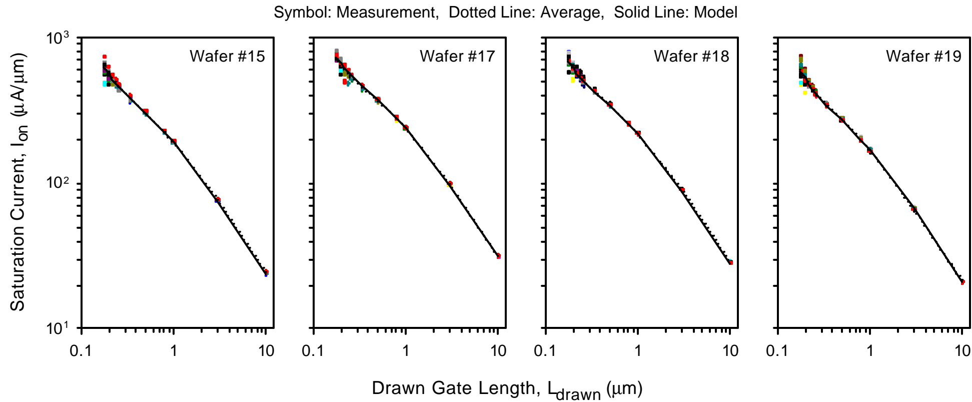

Fig. 3 Predicted saturation currents $I_{on} - L_{drawn}$ (*lines*) through correlation to long-channel V_t with implant dose.

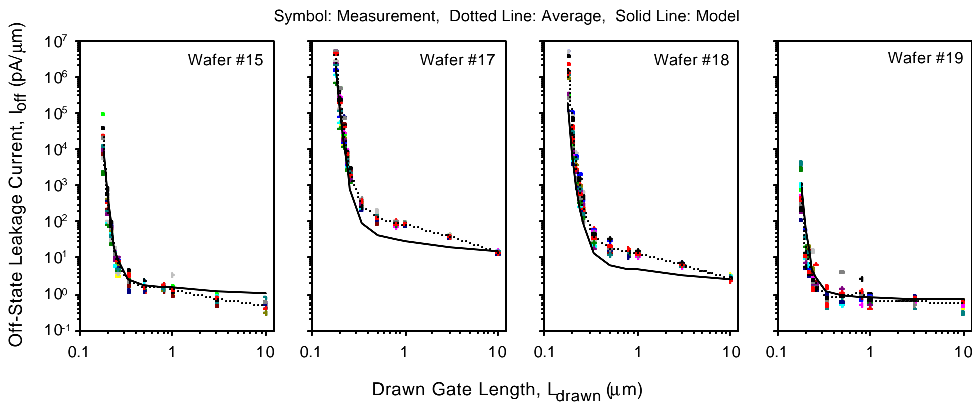

Fig. 4 Predicted leakage currents $I_{off} - L_{drawn}$ (*lines*) through correlation to long-channel V_t and I_{s0}.