A predictive length-dependent saturation current model based on accurate threshold voltage modeling

Khee Yong Lim*, Xing Zhou*, and David Lim†
*School of Electrical & Electronic Engineering, Nanyang Technological University,
Nanyang Avenue, Singapore 639798. *Fax*: (65) 791-2687. *Email*: exzhou@ntu.edu.sg
†Chartered Semiconductor Manufacturing Ltd., 60 Woodlands Industrial Park D, Street 2, Singapore 738406

This paper presents a compact length-dependent saturation current (I_{dsat}) model for deep-submicron MOSFET's based on accurate modeling of the threshold voltage (V_{th}). A predictive bias-dependent V_{th} model that relates to process conditions has been developed [1], [2]. An extension of the V_{th} model [1] is used in this work, which consists of only five important process-dependent parameters and two auxiliary DIBL parameters, namely, N_s, l, a, b, k and i, j, respectively. Each parameter has its own physical representation that characterizes the individual short-channel effects. The first parameter N_s represents an effective vertical channel nonuniform doping profile, whereas the parameters k and b characterize the reverse short channel effect (V_{th} roll-up). The normal short channel effect (V_{th} roll-off) is modeled by l and a. The auxiliary parameters i and j are introduced in this work to fine tune the DIBL dependence, which model the asymmetric nature of the source and drain depletion region at high V_{ds} condition. The V_{th} model requires a five-steps parameter extraction based on only five sets of measurement data: $V_{th}(V_{bs})$ at long channel, $V_{th}(L_g$, low V_{ds}, high $V_{bs})$, $V_{th}(L_g$, low V_{ds}, low $V_{bs})$, $V_{th}(L_g$, high V_{ds}, low $V_{bs})$, and $V_{th}(L_g$, high V_{ds}, high $V_{bs})$. With additional long-channel $V_{th}(V_{bs})$ data for different wafers, the V_{th} model can correlate to process variables such as V_{th} adjust implant dose and punchthrough implant energy.

Once a good V_{th} model is available, developing an I_{dsat} model is mainly a matter of mobility and series resistance modeling. The I_{dsat} model in [3] is employed, combined with our V_{th} model to predict experimental data from the same wafer. The I_{dsat} model considers all the important short-channel effects, which include mobility degradation, velocity saturation, as well as source/drain series resistance. The low-field mobility (m_0) and series resistance (R_s) are extracted by fitting to one set of I_{dsat} versus L_g data at $V_{ds}=V_{gs}=V_{dd}$. Once these two parameters are determined, a complete compact I_{dsat} model with drawn gate length (L_g), bias voltages (V_{gs}, V_{ds}, V_{bs}) and process variables (implant dose f and energy E) as input parameters is available.

The excellent prediction of the I_{dsat} model (lines) to the experimental data (symbols) has been demonstrated in Figs.1-4. The extracted empirical correlation between the channel doping parameter (N_s) and the implant dose and energy (shown in the insets of Figs. 3 and 4) applies equally well to the saturation current. This work demonstrates an efficient and accurate approach to modeling deep-submicron MOSFET's, which is very useful for reducing experimental wafer spilt-lot and for process control and optimization.

[1] X. Zhou, K.Y. Lim, and D. Lim "A General Approach to Compact Threshold Voltage Formulation Based on 2-D Numerical Simulation and Experimental Correlation for Deep-Submicron ULSI Technology Development", submitted to *IEEE Trans. Electron Devices*.

[2] K. Y. Lim, X. Zhou, D. Lim, Y. Zu, H. M. Ho, K. Loiko, C. K. Lau, M. S. Tse, and S. C. Choo, "A predictive semi-analytical threshold voltage model for deep-submicron MOSFET's," *Proc. 1998 Hong Kong Electron Devices Meeting*, Aug. 1998, pp. 114-117.

[3] K. Chen, H. C. Wann, J. Duster, D. Pramanik, S. Naraini, P. K, Ko and C. Hu, "An accurate semi-empirical saturation drain current model for LDD N-MOSFET", *IEEE Electron Device Letters*, vol. 17, no. 3, pp. 145-147, 1996.

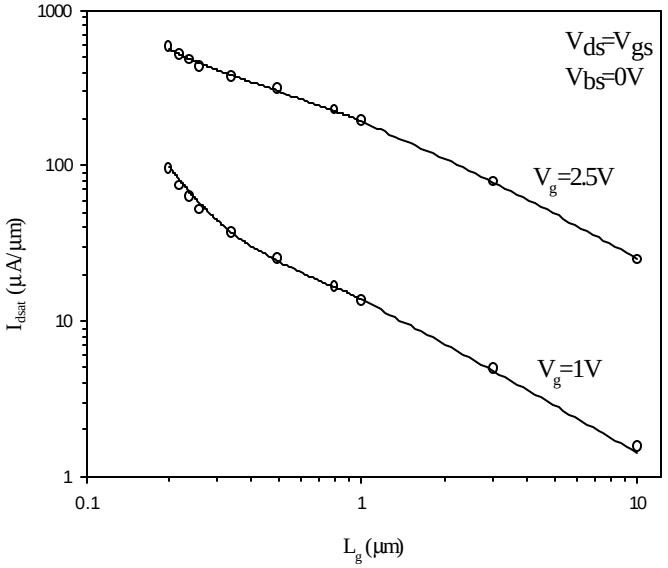

Figure 1: Measured (symbols) and modeled (lines) saturation current vs. gate length for different gate bias. Only the $V_{gs}=V_{ds}=2.5V$ data are used for m_0 and R_s extraction. All others are predictions by the model.

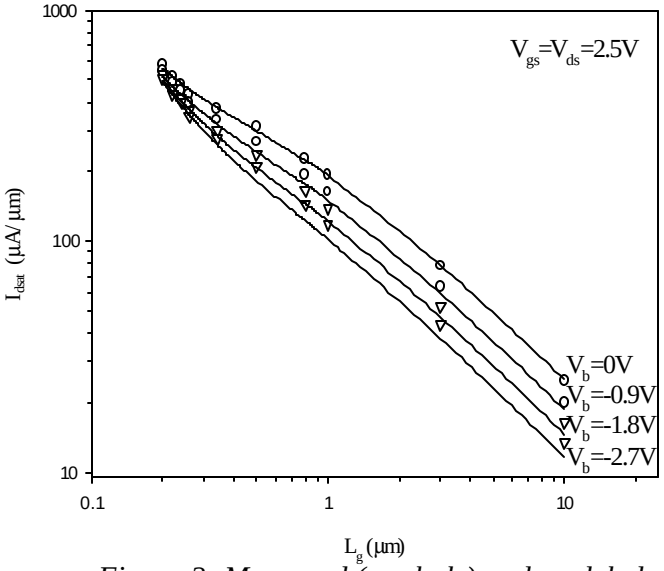

Figure 2: Measured (symbols) and modeled (lines) saturation current vs. gate length for different substrate bias. The V_{bs} dependency is modeled by the parameters within the V_{th} model.

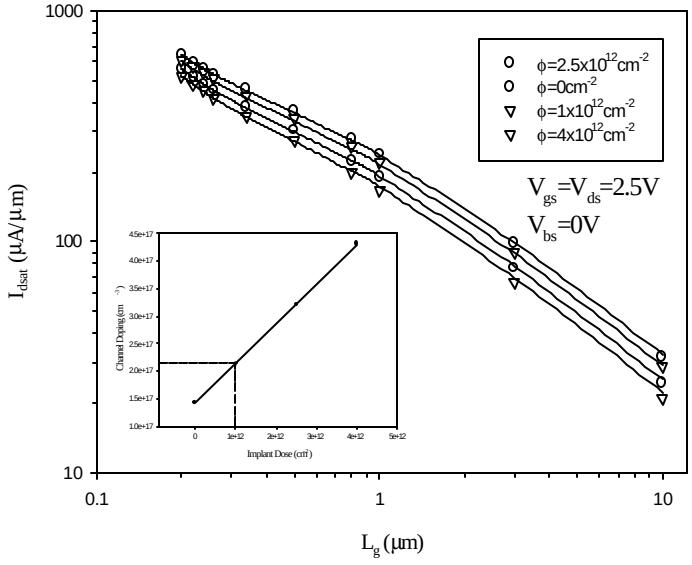

Figure 3: Measured (symbols) and modeled (lines) saturation current vs. gate length for different V_{th} adjustment implant dose. The inset shows the extracted linear correlation between f and N_s.

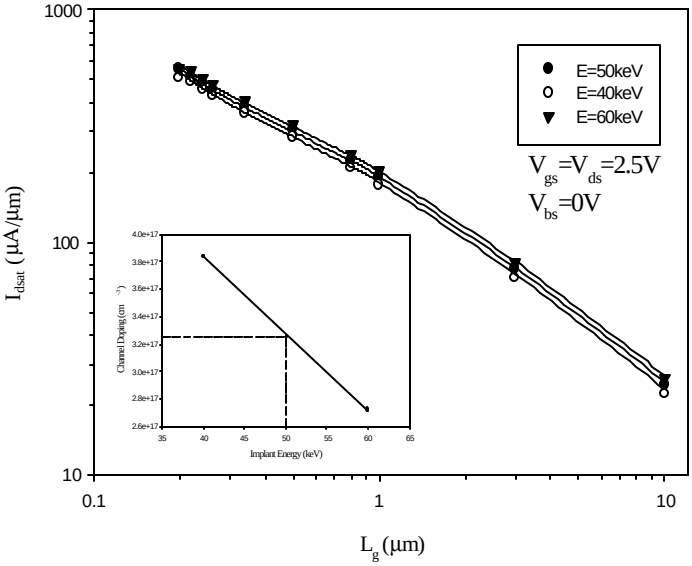

Figure 4: Measured (symbols) and modeled (lines) saturation current vs. gate length for different punchthrough implant energy. The inset shows the extracted linear correlation between E and N_s.