Design Exercise

EE4613: *CMOS Process and Device Simulation*

❑ Objectives

- Design and simulate the processing and characteristics of nMOS transistors for a given 2-μm N-well CMOS process.
- Observe layer structures and profiles at various stages of the process.
- Visualize MOS transistor operation in terms of doping, potential, field, carrier, current distributions.
- Observe and relate device performance parameters to process variations.
- Understand design trade-offs in device performance optimization.
- Learn data analysis and graphical prediction from numerical data.
- Appreciate the differences in analytical and numerical approaches to MOS transistor design.

❑ General Guide [to be applied and carried out during the hands-on sessions]

- Study and understand the given 2-μm N-well CMOS process recipe and mask, TSUPREM-4 commands and VisualFab modules.
- Observe device cross-sectional views at various process steps, probe doping profiles through different cutlines, monitor process parameters (such as oxide thickness, surface/peak doping concentration, junction depth, etc.).
- Emulate *split-wafer experiment* to observe target–variable relations, such as doping profile (and surface/peak doping) versus implant dose and energy, or oxide thickness versus oxidation time and temperature.
- With reference to the given CMOS process recipe, implement the process to simulate only the nMOS transistor of the CMOS process. The resulting structures of your design of experiment (DOE) will be used to investigate the device *scaling characteristics* and performance optimization with *process variations*.
- Review and understand the basic definitions of MOS transistor performance parameters: linear and saturation threshold voltages (V_{t0} and V_{ts}), on-state saturation current (I_{on} or I_{dsat}), off-state leakage current (I_{off}), transconductance (g_{ms}), subthreshold swing (S_{ts}), and drain (output) conductance (g_{ds}).

  Linear threshold voltage: $V_{t0} \equiv V_{gs} \mid I_{ds} = 0$ @ $g_{m0} = \max$ ($V_{ds} = 0.05$V)
  Critical current: $I_{crit} = I_{ds}$ @ $V_{gs} = V_{t0}$ ($V_{ds} = 0.05$ V)
  Saturation threshold voltage: $V_{ts} \equiv V_{gs} \mid I_{ds} = I_{crit}$ ($V_{ds} = 5$ V)
  On-state saturation current: $I_{on} \equiv I_{ds} \mid V_{gs} = V_{ds} = 5$ V
  Off-state leakage current: $I_{off} \equiv I_{ds} \mid V_{gs} = 0,\ V_{ds} = 5$ V
  Transconductance: $g_{ms} \equiv \mathrm{d}I_{ds}/\mathrm{d}V_{gs}$ ($V_{gs} = V_{ds} = 5$ V)
  Subthreshold swing: $S_{ts} \equiv \Delta V_{gs}/\Delta\log(I_{ds})$=1dec (mV/dec) ($V_{ds}$=5V)
  Drain (output) conductance: $g_{ds} \equiv \mathrm{d}I_{ds}/\mathrm{d}V_{ds}$ ($V_{gs} = V_{ds} = 5$ V)

All the above are at zero body bias: $V_{bs} = 0$. For body effect, threshold voltage is defined as: $V_t(V_{bs}) \equiv V_{gs} \mid I_{ds} = I_{crit}$ ($V_{ds} = 0.05$ V, $V_{bs} = -5$ V).

- Run 2D MEDICI simulation on long (10-μm) and short (1-μm) channel transistors to obtain the above-defined device parameters (targets): V_{t0}, V_{ts}, I_{on}, I_{off}, g_{ms}, and S_{ts}. Store the simulation data in the Split Table. Understand the necessary *I*–*V* sweeps to obtain the above parameters.
- Observe and familiarize with the device *I*–*V* characteristics, such as I_{ds}–V_{gs}, log(I_{ds})–V_{gs}, and I_{ds}–V_{ds} in different regions of operation.

➢ Study the **(ideal) theoretical V_t equation** and understand each term in the V_t expression and understand its *functional dependence* on each physical parameter as well as *approximations involved*. Based on the gate work function and fixed oxide charge specifications (in MEDICI) and the resulting structure (i.e., gate oxide thickness t_{ox} and channel doping profile):

- Estimate the "average" channel doping level [how?] and use this average doping to calculate the long-channel threshold voltage V_{t0}. Compare the calculated V_{t0} with that from the numerical device.
- What is the "effective" channel doping (N_{eff} or N_A as used in the ideal V_t equation) that would give the same V_{t0} from the equation as that from the numerical device? Understand the meaning of the "effective" channel doping [and how to obtain it] and the approximations involved.

- Understand "V_{t0} roll-off" and the simple **"triangle"** ***charge-sharing model***.
- Understand the transistor linear/saturation (drift + diffusion) current equations and the main parameters (threshold voltage, transconductance, subthreshold swing), and their relations to oxide thickness and channel doping.
- Study the *transistor I–V characteristics*: understand functional (or behavioural) dependence of I_{ds} on V_{gs} at low and high V_{ds}, and influence of V_{t0}, V_{ts}, g_m, and S_t on I_{on}, I_{off}. Observe, analyze, and understand the basic behaviours ("shapes") of I_{ds}–V_{gs} for:
  - Linear (@ V_{d0}) vs. saturation (@ V_{dd}) I_{ds} on linear scale;
  - Linear (@ V_{d0}) vs. saturation (@ V_{dd}) I_{ds} on log scale;
  - Long-channel vs. short-channel I_{ds} on linear/log scales.
- Study the *transistor scaling characteristics*: device parameters (V_t, I_{on}, I_{off} as well as g_m and S_t) as a function of decreasing gate length, L_g.
  - Write a simple program (Excel, Matlab, C) to plot "V_t vs. L_g" curves based on the theoretical V_t equation (long-channel) and "triangle" charge-sharing model (short-channel) with a given set of *transistor parameters* (N_A, t_{ox}, Φ_m; x_j). Vary and observe the "V_t vs. L_g" changes by changing parameter values.
  - Obtain MEDICI device structures of different gate lengths using structure truncation/reflection (Recommended: L_g = 10, 5, 2, 1.6, 1.2, 1, 0.8, [0.7] μm). Note the metallurgical ("effective") channel length $L_{ch} = L_g - 2\sigma x_j$ (where $\sigma \sim 0.7$) is due to n^+ source/drain lateral diffusion.

– Obtain *technology optimization curves*, e.g., V_{t0}–log(L_g), V_{ts}–log(L_g), g_m–log(L_g), S_t–log(L_g), I_{on}–log(L_g), log(I_{off})–log(L_g), and log(I_{off})–I_{on}. Compare with theoretical calculations, e.g., V_{t0} "roll-off" based on the simple "triangle" *charge-sharing model*. Determine minimum gate length based on a given set of criteria; or alternatively, determine various performance parameters at a given "designed" gate length.

❑ **Exercise** [practice through examples to reinforce the concepts and relate to analytical theory]

➢ Through DOE, split wafer with selected process variations. Observe and optimize the device performance through **target–variable relationship**. Use analytical theory as a guide to relate target–variable dependencies and learn *graphical solutions* (numerical interpolation) for data analysis.

➢ Determine *new* process variables for improved "on/off" current trade-off for logic-circuit applications. Specifically, tune the given ("original") process such that for the **designed L_g = 1 μm device**, drive current (I_{on}) can be increased AND leakage current (I_{off}) can be reduced, with the guide that the linear threshold voltage at L_g = 1 μm is *relatively* unchanged. Below are some examples of DOE's you may follow.

– With reference to the long-channel (10-μm) and short-channel (1-μm) devices, run separate DOEs for V_t-adjustment implant *Dose* (Φ) variations at a given gate-oxidation *Time* (t) and t variations at a given Φ, respectively, to observe the trend in "V_{t0} roll-off" ($\Delta V_{t0} = V_{t0_10\mu m} - V_{t0_1\mu m}$) and "drain-induced barrier lowering (DIBL)" ($\Delta V_{DIBL} = V_{t0_1\mu m} - V_{ts_1\mu m}$) as a function of t (or t_{ox}) as well as a function of Φ (or N_A). [*Question*: Can you do some calculations as a guide?]

– Based on the ideas in reducing the two major short-channel effects, namely, "ΔV_{t0} roll-off" and "ΔV_{DIBL}", decrease t_{ox} (by decreasing gate oxidation *Time*, t) and increase N_A (by increasing V_t-adjustment implant *Dose*, Φ), while maintaining the same V_{t0} for the L_g = 1 μm device.

– Based on the best-estimated (Φ and t) combination, run the "full-loop" for various gate-length devices in comparison with the original process. Plot *technology curves* for the "new" process with respect to the "original" process, such as **V_{t0} and V_{ts} vs. log(L_g)**; g_{ms} vs. log(L_g); S_{ts} vs. log(L_g); I_{on} vs. log(L_g); log(I_{off}) vs. log(L_g); and **log(I_{off}) vs. I_{on}**.

– Alternatively, run "full-loop" DOE on the "nominal" (1-μm) device for various Φ and t combinations, and plot the *"scattered" optimization data* such as log(I_{off}) vs. I_{on}, S_{ts} vs. g_{ms}, V_{ts}, vs. V_{t0}. Identify the best (Φ and t) condition and understand the reason from S_{ts}–g_{ms} and V_{ts}–V_{t0} data.

– *Optional*: consider other process variables, such as punch-through (PT) implant dose/energy; or n^+ source/drain implant dose/energy.

– Collect relevant data to explain why your new process is better than the original given process. Relate the process variations to the reduction of major short-channel effects.

– Once certain improvements are made, find out the reasons and follow similar approaches to see if you can further optimize the process to improve the performance (i.e., take your new process as "nominal");

therefore, to understand how the I_{on} and I_{off} are dependent on the device and process parameters and how they can be both improved.

- ***Major concepts to be learned***:
  - Technology generations and major *short-channel effects* (V_t roll-off and DIBL), and ways to reduce them.
  - Device optimization parameters (I_{on} and I_{off}) and their relations to process variables (Φ and t) via device electrical parameters (V_t, g_m, S_t) and structural parameters (t_{ox}, N_{eff}, x_j).

❑ Notes

- Study the design and plan your experiments. Apply the basic theory you have learned as a guide. Be aware that you have limited time and disk space for the project, and try to make the best use of hands-on sessions.
- Concentrate more on making observations from numerical data, knowing alternatives, applying knowledge, observing discrepancies, analyzing and explaining results, and your creative thinking. Design your experiments with specific objectives. It is more important to demonstrate *the approach* you are taking than simply arriving at a solution.
- Learn to "sketch" device behaviors (e.g., I_{ds}–V_{gs}, V_t–L_g, I_{off}–I_{on}) at various bias conditions, geometries, oxide, and doping variations. The shapes of these curves (linear or log scale, long or short, linear or saturation) contain essential physics, and how you draw them, reflects your understanding.
- ***Report writing***: Writing report is the final, but very important, stage of a learning process. It is the opportunity for you to re-organize your logical reasoning in your design, and present and demonstrate your understanding on the subject. The process of writing the report is itself a learning process, in which you can reinforce the knowledge and experience you have learned in the design. More questions will be given during class. Some specific notes:
  - Include only those "necessary" plots to support your analysis. It is best to include your own questions that you have learned/answered.
  - One "brief" report is to be handed in per person. It is essentially *reporting your understanding* of this Design. No need for detailed theory — only present what you have done and learned. Hand-written with sketches and annotations on plots are encouraged.
- ***This is an <u>open-ended</u> design exercise. Take this assignment as a <u>guide</u> rather than trying to 'answer' listed questions.*** *Also, take this exercise as an <u>opportunity</u> to do something different from your past year experience —* ***explore with your own creative thinking****.* Your performance and report will be evaluated at the following three levels:
  - **Solution**: The ability to arrive at a solution to the given problem [C~B].
  - **Approach**: The ability to analyze with reasoning in *your approach* [B~A].
  - **Creativity**: The ability to *raise questions* and solve them; and demonstration of your understanding on what is taught, and application to solving problems *beyond* what is taught [A^+].