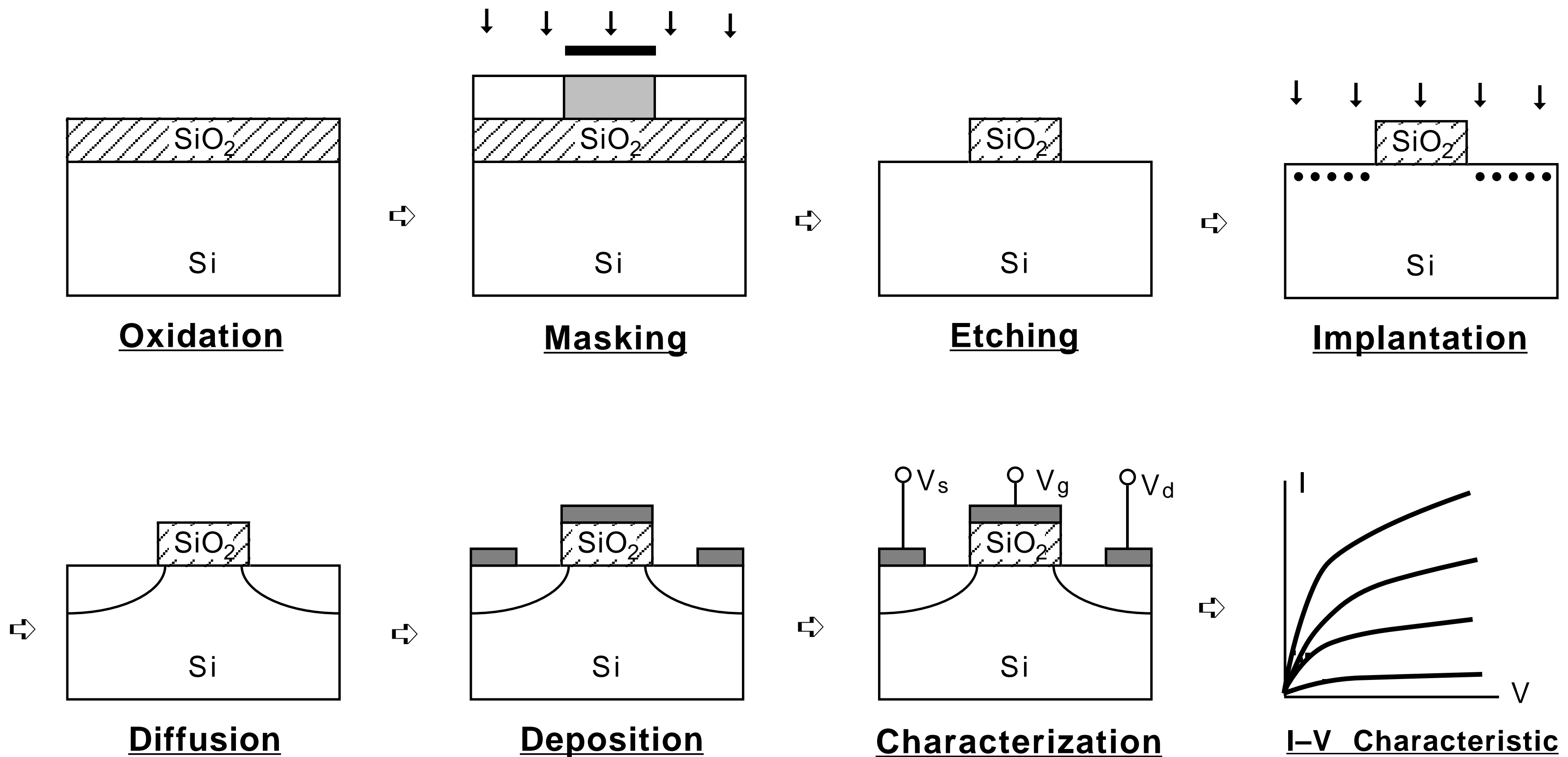
Major Process Steps — A Simplified View



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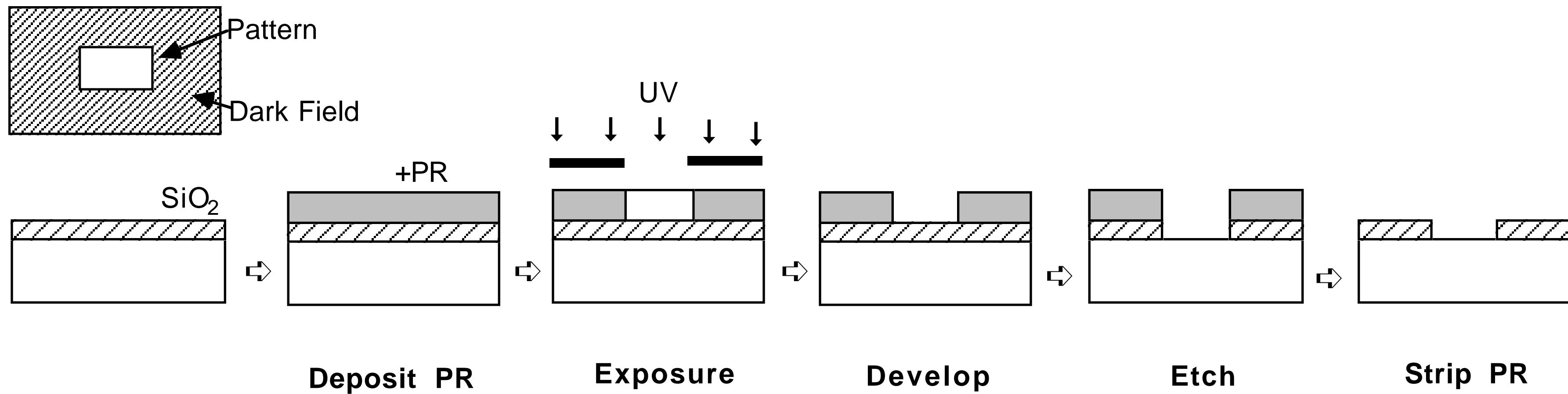
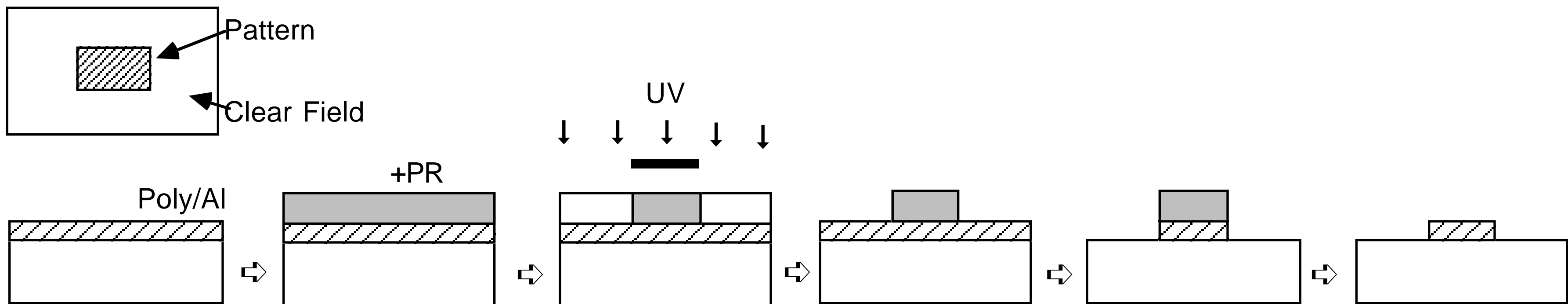
Masking and Photolithography





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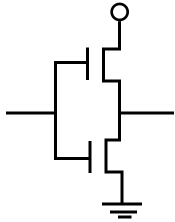
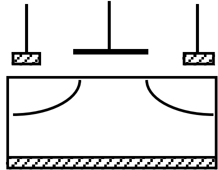
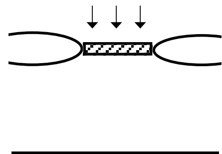
CMOS Device Design Considerations

	Variables	**Targets**
Circuit 	• SPICE: V_{T0}, KP, λ, γ, … • Geometrical: L, W • Electrical: V_{dd}, V_{sub}	• Digital: t_r, t_f, t_d, P_d, I_{dsat}, BV, NM • Analog: g_m, g_d, f_T, f_{max}, A_V
Device 	• Physical: t_{ox}, x_j, $N(x)$, R_{sh} • Model: μ, τ, …	• Electrical: V_T, I_{dsat}, g_m, g_d, C_g, BV, W_d, L_{eff} • Physical: $\psi(x)$, $E(x)$, $J(x)$, $v(x)$, $n(x)$, $p(x)$
Process 	• Process: T, t, E_0, Φ_0, P_{H_2O}, ambient • Model-related	• Layer: t_{ox}, x_j, R_{sh} • Profile: $N(x)$, N_{surf}, N_{peak}, R_p, ΔR_p • Structure-related

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Mask Design Considerations

❑ Objective of simulation

- Short-channel electrical performance — use full FET structure (truncation/ reflection will not be accurate)
- Device performance due to structural variation — mask should include the necessary changes (e.g., channel length; gate–drain spacing of an LDD)

❑ Trade-off between grid points and design rule

- Well–active separation: well lateral diffusion vs field oxide dimension

❑ Optional mask levels

- Certain masks can be omitted with the use of negative photoresist or other films as mask in process simulation

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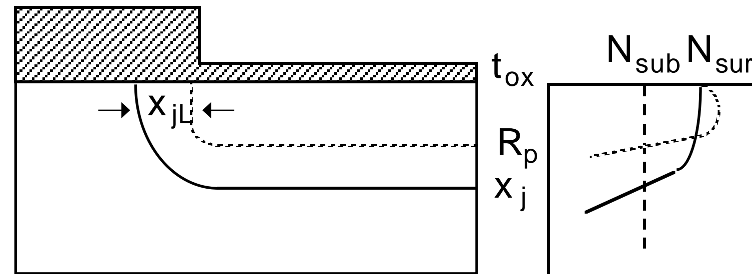
Well Design Considerations



❑ Parameters

- Well doping: $\overline{N}_{well}$
- Surface concentration: N_{surf}
- Junction depth: x_j
- Lateral diffusion: x_{jL}

❑ Dependencies

- $\overline{N}_{well}(\Phi)$
- $N_{surf}(\Phi, R_p(E), t_{ox}(t_{pad}, T_{pad}))$
- $x_j(t_{drv}, T_{drv}, R_p(E), N_{sub})$
- $x_{jL}(t_{drv}, T_{drv}, R_p(E))$

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Well Design Considerations

❑ Well doping

- $\overline{N}_{well} > (5\text{–}10) N_{sub}$ for PMOS control
- $\overline{N}_{well}$ too high: $\left\{ \begin{array}{l} \text{back-gate bias sensitivity} \\ \text{excessive-doping effect } (\mu \downarrow) \\ C_{S/D-well} \uparrow \end{array} \right.$

❑ Surface concentration

- $N_{surf} \uparrow (\Phi \uparrow)$: $\left\{ \begin{array}{l} \text{improve PMOS punch-through performance} \\ \text{no need for channel stop in N-well field oxide} \end{array} \right.$

❑ Junction depth and lateral diffusion

- $R_p \uparrow (E \uparrow)$: $\left\{ \begin{array}{l} \text{less thermal cycle } (x_{jL} \downarrow) \\ \text{increased packing density} \end{array} \right.$

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Source/Drain Design Considerations

❑ Design parameters

- Junction depth: x_j, x_{jL}
- Doping level and profile: N_{surf}

❑ Design variables

- S/D implant dose and energy
- Annealing temperature and time
- Gate oxide thickness (gate oxidation temperature and time)

❑ Design considerations

- Short-channel effect: $L_{eff} = L - \sqrt{2\varepsilon_{ox}\varepsilon_{Si}/(qN_{sub})\,[V_{DS} - (V_{GS} - V_T)]}$
- Hot-electron effect: $\mathcal{E}_{max}$ (“drain engineering” — LDD)

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Threshold Design Considerations — Definition

$$V_T \equiv V_G \big|_{\phi_s = 2\phi_F} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} + 2\phi_F - \frac{Q_{sub}}{C_{ox}}$$

❑ Basic terms

- Gate capacitance: $C_{ox} = \varepsilon_{ox}/t_{ox}$
- Fermi potential: $\phi_F = \frac{kT}{q} \ln\left(\frac{\overline{N}_{sub}}{n_i}\right)$
- Flat-band voltage: $V_{FB} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}}$
- Workfunction: $\phi_{MS} = \phi_{F(\text{poly})} - \phi_{F(\text{Si})}$
- Oxide charge: $Q_{ox} = Q_f + Q_I + Q_{ss} = t_{ox} \int_0^{t_{ox}} x\rho_{ox}(x)\, dx$
- Depletion charge: $Q_{sub} = -\sqrt{2q\varepsilon_{Si}\overline{N}_{sub}(V_{SB} + 2\phi_F)}$

❑ Alternative form

$$V_T = V_{T0} + \gamma\left[\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right];\ \gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{Si}\overline{N}_{sub}}\ ;\ V_{T0} = V_T\big|_{V_{SB}=0}$$

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Threshold Design Considerations — Extraction

- **Linear region**: $V_{GS} > V_T + V_{DS}$ (i.e., $V_{DS} << \phi_s$)

$$I_{DS} = \beta\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \approx \beta(V_{GS} - V_T)V_{DS};\ \beta = \mu C_{ox}\left(\frac{W}{L_{eff}}\right)$$

$$V_T = \frac{V_{GS1} - (I_{DS1}/I_{DS2})V_{GS2}}{1 - I_{DS1}/I_{DS2}};\ V_T = 2V_{GS1} - V_{GS2}\ (\text{if } I_{DS2} = 2I_{DS1})$$

- **Saturation region**: $V_T < V_{GS} < V_T + V_{DS}$

$$\sqrt{I_{DS}} = \sqrt{\frac{\beta}{2}}(V_{GS} - V_T)$$

$$V_T = \frac{V_{GS1} - \sqrt{I_{DS1}/I_{DS2}}V_{GS2}}{1 - \sqrt{I_{DS1}/I_{DS2}}};\ V_T = 2V_{GS1} - V_{GS2}\ (\text{if } I_{DS2} = 4I_{DS1})$$

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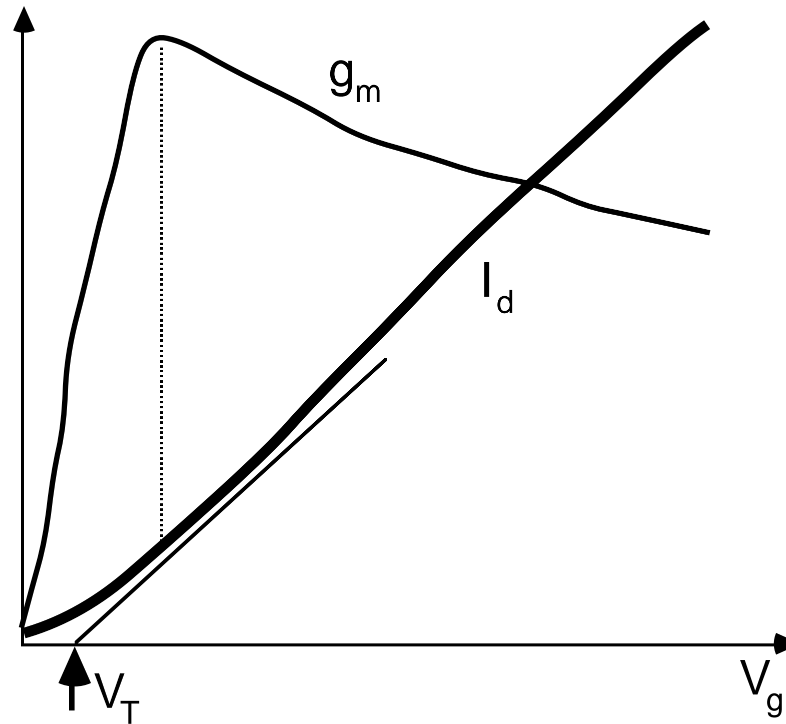
Threshold Extraction from Simulation



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Threshold Design by Simulation

❑ Theoretical approach

- What is the meaning of an "effective substrate doping," $\overline{N}_{sub}$?
- Is the square-root law really accurate?
- What is ϕ_F from an experimental point of view?

❑ Simulation approach

- Based on the intercept of the simulated inversion charge Q_n (or sheet conductance G_s) vs V_{GS} and the extrapolation of the linear part of the I_{DS}–V_{GS} curve

$$G_s = \frac{1}{R_s} = \frac{I}{V}\frac{L}{W} \Rightarrow I_{DS} = G_s \frac{W}{L} V_{DS} \text{ (assuming small } V_{DS}\text{)}$$

- Similar approach to obtaining threshold voltage from measured I–V data
- Simulated "data" (Q_n–V_{GS}) are obtained by solving semiconductor equations with arbitrary doping profiles, independent of the above assumptions

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Threshold Design Considerations

❑ Threshold dependencies

- Body bias (γ, V_{SB})
- Substrate doping (Q_{sub}, ϕ_F)
- Temperature (Q_{sub}, ϕ_F, n_i, E_g)
- Material (ϕ_{MS}, $C_{ox}(\varepsilon_{ox})$, Q_{ox}(orientation))

❑ Design variables and trade-offs

- Constant shifts: ϕ_{MS}, Q_{ox}
- "Fixed" (scaling rule): t_{ox}
- Key parameter: *channel doping*: $N_{ch} \begin{cases} \text{too high} - \mu \downarrow \\ \text{too low} - \text{punch-through} \end{cases}$
- Use shallow implant to adjust V_T, and deep implant to prevent punch-through

$$\left.\begin{array}{r} \phi_{MS} \\ Q_{ss};\ Q_f \\ t;\ T \rightarrow\ t_{ox} \end{array}\right\} \boxed{V_T} \begin{cases} \Phi_{V_T};\ E_{V_T} \\ N_{sub} \text{ or } N_{well} \leftarrow \Phi_W;\ E_W \\ L_{eff} \leftarrow \Phi_{S/D};\ E_{S/D} \\ \text{after thermal cycles } (t;\ T) \end{cases}$$

❑ Circuit requirements — NM, I_{dsat}, g_m, f_T, etc.

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Relate Circuit/Device Performance to Process Variations

- ***In principle, any circuit/device performance parameter can be related to process variables. The question is: how are they related?***

❑ **Analysis**

- Start with definitions
- Find appropriate analytical formulations
- Relate physical parameters to process variables

❑ **Trade-off**

- Study design/technology constraints and parameter ranges
- Identify conflicting conditions

❑ **Optimization**

- Find the "process window" through numerical simulation
- Optimize targets using DOE and RSM

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Example: Unity Current Gain Cutoff Frequency

$$f_T = \frac{g_m}{2\pi C_G}$$

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}}\bigg|_{V_{DS}} = \begin{cases} \beta V_{DS} \text{ (linear)} \\ \beta(V_{GS} - V_T) \text{ (saturation)} \end{cases} \qquad \beta = \mu C_{ox} \frac{W}{L_{eff}}$$

$$C_G = C_{GB} + C_{GS} + C_{GD} = f(C_{ox}, L_{eff}, N_{sub}, V_{GS}, V_{DS}) \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

- t_{ox}: Gate oxidation temperature, time, ambient, etc.
- μ: Substrate doping (well implant dose and energy), etc.
- L_{eff}: S/D implant dose and energy, annealing temperature and time, gate oxide thickness, channel doping, etc.

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