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Optimization of design and fabrication for micromachined true time delay (TTD) phase shifters

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Abstract

Distributed techniques have been widely employed as a solution to obtain wide band circuits at microwave and millimeter wave band. This paper presents five different designs for true-time delay (TTD) phase shifters that are based on characteristic impedance of 75, 65 and 50 Ω coplanar waveguide (CPW) distributed microelectromechanical systems (MEMS) transmission line (DMTL), which are loaded with different designs and number of shunt capacitive switches. The TTD phase shifters are fabricated on a 675 μm high resistivity silicon (Si) wafer using surface micromachining process. The design operates up to Ku band with a measured return loss below −15 dB and an average loss of 2.3 dB/phase shift of 250° at 20 GHz. The TTD phase shifters have wide applications for high-performance of microwave and millimeter-wave integrated circuits.

Keywords: MEMS; Capacitive shunt switch; Distributed MEMS transmission line (DMTL); True time delay (TTD) phase shifter; Radio frequency (RF)

1. Introduction

Current development in radio frequency (RF) microelectromechanical systems (MEMS) has greatly improved the performance of the millimeter wave switches and phase shifters, which are essential for modern radar and telecommunication systems. Low loss and less measurable intermodulation distortion are two main advantages of MEMS over field effect transistor (FET) or p-i-n diodes [1]. As a result, RF MEMS concept has been successfully applied in the past few years to develop low loss RF switching devices and variable capacitors [2–4]. Most of these MEMS based switches can be fabricated directly with on quartz, glass and silicon substrates, which results in a relatively low-cost phased array antenna [5,6]. Although the switching speed of the MEMS devices may not be comparable to the FET or p-i-n diodes switches, the MEMS devices have better performance in terms of isolation and insertion loss at millimeter-wave frequencies.

There are two classes of RF MEMS phase shifters namely analog and digital. The analog phase shifters provide a continuous variable phase shift from 0 to 360° using varactor capacitive switches [7]; whereas the digital phase shifters provide a discrete or quantized set of phase delays with 1 bit 180°, 2 bit 180°/90° set of delay networks which allow phase shifts of 0, 90, 180 and 270° depending on the combination of bits used [8]. When comparing to the other topologies, the distributed MEMS transmission line (DMTL) phase shifter on silicon wafer proposed in this paper has the advantage of low cost, low loss and small size. In addition, the DMTL phase shifters demonstrated in this work have better performance [9] on simple coplanar waveguide (CPW) transmission lines because CPW based phase shifters are uniplanar. This is one of the main advantages as only one side of the substrate is used; eliminating the need for via-hole process and simplifying the fabrication and integration process with other components. When a single analog control bias voltage is applied to the center conductor, the bridges will be pulled closer to the center conductor, which in turn increases the loading capacitance in the switch, besides varying the

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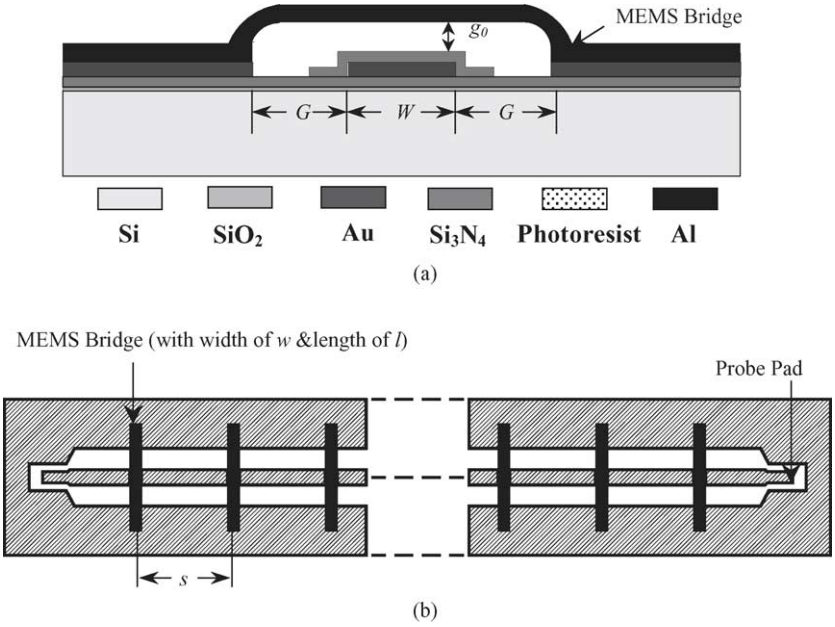

Fig. 1. The configuration for (a) cross sectional view of MEMS shunt switch over CPW transmission line and (b) DMTL.

propagation characteristics and decreasing the phase velocity of the DMTL. The resulting change in the phase velocity of the DMTL produces the TTD phase shifts. This paper analyzes five different designs of DMTL phase shifters based on simple CPW transmission lines and the objective is to optimize the designs with low cost and size, and maximize phase shift per dB loss by varying the impedance size of the transmission lines and the number of switches developed on silicon wafer.

The structure of this paper is organized as follows. Section 2 describes the design of the DMTL phase shifter that covers the designs of single switch and the different types of CPW transmission line. Section 3 provides the fabrication processes of the shunt capacitance switch and the DMTL phase shifters. Section 4 reports the experimental results and discusses the different design of the DMTL phase shifters. Section 5 presents conclusions on the findings.

2. The architecture of the DMTL phase shifter

The DMTL phase shifter consists of a high impedance (>50 Ω) CPW transmission line and MEMS shunt switches that are loaded by the periodic placement of variable capacitance. The configuration of the MEMS shunt switch over the CPW transmission line is shown in Fig. 1. W is the CPW center conductor width, G the CPW gap width, g_0 the bridge height, s the periodic spacing of the MEMS bridges on the CPW line, w and l are the width and length of the MEMS bridge, respectively. The DMTL is connected to 50 Ω input and output lines to match with probe pads.

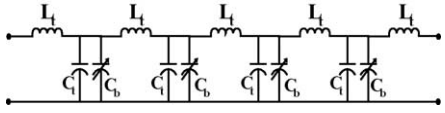

Fig. 2. Equivalent circuit of the loaded DMTL.

2.1. Loss versus impedance

An equivalent circuit of the MEMS bridge over the transmission line is shown in Fig. 2, which consists of variable shunt capacitor, C_b of bridge, the per unit length capacitance, C_t and the inductance, L_t of the unloaded CPW transmission line is given by [10].

$$C_t = \frac{\sqrt{\varepsilon_{reff}}}{cZ_0} \tag{1a}$$

$$L_t = C_t Z_0^2 \tag{1b}$$

where ε_{reff} is the effective dielectric constant, Z_0 the characteristics impedance of the unloaded transmission line and c is the free space velocity. The characteristic impedance, Z_l and phase velocity, v_l of the loaded line are given by

$$Z_l = \sqrt{\frac{L_t}{C_t + C_b/s}} \tag{2a}$$

$$v_l = \frac{1}{\sqrt{L_t(C_t + C_b/s)}} \tag{2b}$$

The loaded line is designed such that $Z_l \approx 50\ \Omega$ by choosing an unloaded line impedance of $Z_0 > 50\ \Omega$.

The Bragg frequency is the frequency at which the characteristic impedance of the line goes to zero, where entire power reflects back. In the case of the DMTL, the

up-state inductance–capacitance (LC) resonant frequency of the MEMS bridges is very high (300–600 GHz). As a result, the operation is generally limited by the Bragg frequency f_{Bragg} of the loaded line. The Bragg frequency is given by

$$f_{\text{Bragg}} = \frac{1}{\pi s\sqrt{L_t(C_t + C_b/s)}} \tag{3}$$

In order to determine the width of the optimal center conductor and the associated unloaded line impedance, both the phase shift and the loss contributed by the loaded line against center conductor width must be determined. The phase shift of the DMTL is determined by the impedance change, which also determines the reflection coefficient of the phase shifter. The phase shift $\Delta\phi$ of this slow wave structure can be calculated by

$$\Delta\phi = \omega\sqrt{L_tC_t}\left(\sqrt{1 + \frac{C_{lu}}{sC_t}} - \sqrt{1 + \frac{C_rC_{lu}}{sC_t}}\right) \tag{4}$$

By substituting the Eqs. (1a), (1b), (2a) and (2b) into (4), the following expression is derived as

$$\Delta\phi = \frac{\omega Z_0\sqrt{\varepsilon_{\text{reff}}}}{c}\left(\frac{1}{Z_{ld}} - \frac{1}{Z_{lu}}\right) \tag{5}$$

where Z_{lu} and Z_{ld} are the loaded-line impedance values at the up- and down-state, respectively. The effective capacitance seen by the DMTL at the up-state is C_{lu}, at the down-state is C_{ld} and C_r is capacitance ratio. The impedance varies when the loss of the transmission line is changed due to a change in the amount of capacitance on the transmission line. In order to achieve the maximum amount of phase shift for the minimum amount of insertion loss, the attenuation constant α for the unloaded CPW transmission line can be expressed as [11]

$$\alpha = \beta\frac{8.86\times10^2 R_s\sqrt{\varepsilon_{\text{reff}}}}{4\eta_0 SK(k)K(k')(1-k^2)} \times\left[\frac{2S}{W}\left\{\pi + \ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right\} +2\left\{\pi + \ln\left(\frac{4\pi S(1-k)}{t(1+k)}\right)\right\}\right] \tag{6}$$

$$\alpha_l = \alpha\frac{Z_0}{Z_{ld}} \tag{7}$$

$$R_s = \sqrt{\frac{\pi f\mu_0}{\sigma}} \tag{8}$$

where α_l is the loaded line attenuation constant, R_s the surface resistance, t the metal thickness, β the correction of multiplicative factor, η_0 the characteristic impedance of free space, f the frequency, W the width of the CPW center conductor, G the width of the CPW gap, σ the conductivity of the metal, k the modulus of elliptical integral, k' the complementary modulus of k for the elliptical integral, $K(k)$ and $K(k')$ are the complete elliptic integral of the first kind of modulus k and complete elliptic integral of the first kind of complementary modulus k', respectively.

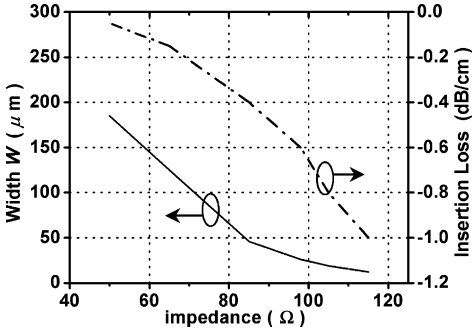

Fig. 3. The line losses and width vs. impedance on Si substrate for ($W + 2G = 450\ \mu$m).

Another important factor which required careful consideration is the radiation loss. It is present in an unloaded CPW line on a thick dielectric substrate. This is because the wave velocity of the transmission line being greater than the phase velocity of the waves in the dielectric. The loaded line is built on low dielectric constant substrates (quartz or GaAs), the wave velocity of the transmission line is slower than the phase velocity in the dielectric and radiation loss cannot occur. Thus, the line loss per unit length on silicon substrate is higher than that on quartz substrate. The CPW transmission line loss with impedance on silicon substrate is shown in Fig. 3. It is also important to select the input and output port feed lines to match the dimensions and minimize the radiation loss in these lines.

2.2. Design of single switch

The capacitive MEMS shunt switch is important in the design of the DMTL phase shifter. The capacitive shunt switches [12] are developed on CPW transmission line with different values of characteristic impedances namely, 75, 65 and 50 Ω. A 675 μm high resistivity silicon substrate with 1.5 μm thick gold (Au) metal, 1500 Å of Si_3N_4 dielectric layer is used to insulate the dielectric between the aluminum (Al) material bridge and the CPW transmission line. The aluminum material bridge, which has length of 700 μm, width of 90 μm and thickness of 1.5 μm, is suspended above the CPW transmission line with a 2 μm gap. Fig. 4a and b shows the simulated results of the switches at their up- and down-state using the high frequency structure simulator (HFSS) system software [14]. These results show that high impedance loaded CPW transmission line have more superior performance compared to the low impedance loaded line.

It is desirable to have pull-down within the range of $V_p \leq 40$ V, therefore, a wide center conductor and high unloaded impedance is necessary [16]. For a good compromise, it is required to analyze the electrostatically deformed diaphragms. The mechanical design of the capacitance switch involves the application of electrostatic force to deformable structures. The charges are redistributed during the bridge

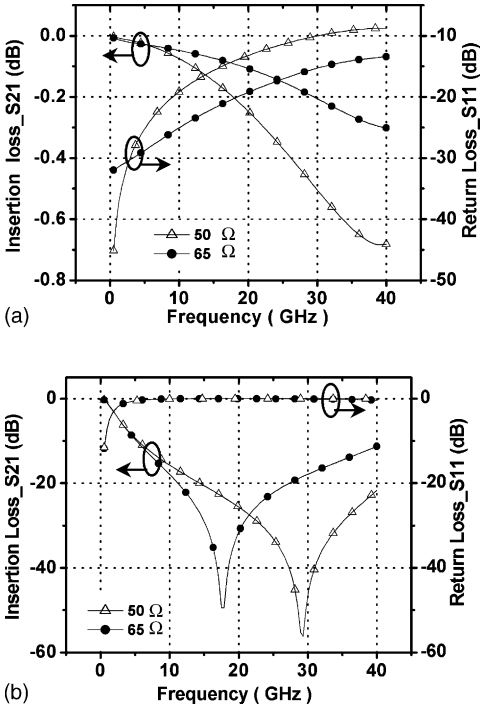

Fig. 4. The simulated results of the switch for both 65 and 50 Ω (a) up-state and (b) down-state.

structure deformation, which in turn modifies the mechanical load. The pull-down force of the switching bridge due to an applied bias on the center conductor of CPW is given by

$$F = \frac{\varepsilon_0 W w}{2g_0^2} V_{\text{bias}}^2 \tag{9}$$

where ε_0 is the free-space permittivity and V_{bias} is the applied bias voltage as shown in Fig. 1a. The spring constant k_s of the bridge is approximated by [17]

$$k_s = \frac{32Et^3 w}{(W+2G)^3} + \frac{8\sigma(1-\upsilon)tw}{W+2G} \tag{10}$$

where E is the Young's modulus of the bridge material, t the bridge thickness, σ the internal residual stress of the bridge and υ is the Poisson's ratio. Then, the pull-down voltage, V_p is given by

$$V_p = \sqrt{\frac{8k}{27\varepsilon_0 W w} g_0^3} \tag{11}$$

Various factors should be considered in order to analyze the electro-mechanical problems. A model that can accurately predict the dynamic behavior of the MEMS bridge structure should also integrate with several different phenomena. These phenomena include electrostatics, mechanics, residual stress, contact forces, compressible squeeze film damping and impact effects on a microscale. In this paper, a simple one-dimensional nonlinear model is employed to simulate the dynamic behavior of the switch [18]. The differential motion equation of the bridge can be expressed as

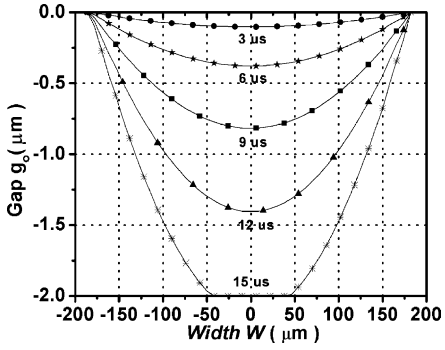

Fig. 5. Changes for the shape of the bridge at different time.

$$mz'' + bz' + K_z z = F_e + F_c \tag{12a}$$

where m is the switch mass, b the damping coefficient, K_z the switch spring constant in the z-direction, F_e the electrostatic force on the switch, and F_c is the contact force when the switch touches the dielectric. The parameters in Eq. (12a) can be summarized as

$$b = \frac{K_z}{\omega_0 Q} \tag{12b}$$

$$F_e = \frac{\varepsilon_0 W w V^2}{2(g_0 - z)^2} \tag{12c}$$

$$Fc = \frac{m1\,Ww}{(g_0 - z)^3} - \frac{m2\,Ww}{(g_0 - z)^{10}} \tag{12d}$$

where w_0 is the resonant frequency and Q is the quality factor.

The pull-down time is calculated based on the assumption that the shape of the deformed bridge remains flat and is independent of its position. Then, the change of the shape of the deformed bridge with the time is simulated and shown in Fig. 5 under a voltage of 40 V. It can be seen from the simulation results, after 15 μs, the bridge touches the surface of the dielectric layer. It should be noted that the bridge membrane and the surface of dielectric layer are assumed to be flat. However, simulation results indicate that the switch pull-down time is around tens of microseconds.

2.3. Design of CPW transmission line

Three types of CPW transmission lines are designed with different impedances on high resistivity silicon wafer. The design parameters of the three types of CPW transmission line are shown in Table 1. In general, these CPW transmission lines differ in terms of their impedances. Phase Shifter-I, Phase Shifter-II and Phase Shifter-III are designed with impedance of 75, 65 and 50 Ω, respectively, where $(W+2G)$ are 400, 450 and 300 μm, respectively. In each of the design, there are 11 shunt capacitance switches, equally spaced at 800 μm and placed above a 10 mm transmission line. It is necessary to have a Bragg frequency of 40 GHz at the maximum capacitive loading [4] and to maintain the loaded line

Table 1
Design parameters of CPW transmission line with experimental results

Design parameter	Phase Shifter-I	Phase Shifter-II	Phase Shifter-III
Impendence, Z_0 (Ω)	75	65	50
Width, $W+2G$ (μm)	400	450	300
Height, g_o (μm)	675	675	675
Frequency, f_B (GHz)	40	40	40
Number of switch	11	11	11
Space, s (μm)	800	800	800
Experimental result			
S_{21} (dB) @ 20GHz	−3.2	−2.0	−3.2
S_{11} (dB) @ 20 GHz	−13	−17	−12
Phase @ 20 GHz	100°	148°	80°

Table 2
Design parameters of DMTL phase shifter with experimental results

Design parameter	Phase Shifter-II	Phase Shifter-IV	Phase Shifter-V
Impendence, Z_0 (Ω)	65	65	65
Width, $W+2G$ (μm)	450	450	450
Height, g_0 (μm)	675	675	675
Frequency, f_B (GHz)	40	40	40
Number of switch	11	11	16
Space, s (μm)	800	500	300
Experimental result			
S_{21} (dB) @ 20 GHz	−2.0	−2.0	−2.3
S_{11} (dB) @ 20 GHz	−17	−18	−15
Phase @ 20 GHz	148°	180°	250°

impedance within the range of 45–53 Ω so that the return loss can be below −15 dB up to Ku band. The simulated results of the various phase shifters which are designed using both HFSS [14] and advanced design system (ADS) [15] system software are shown in Fig. 6. From Fig. 6, the Phase Shifter-II has better and more superior performance than the others in terms of low insertion loss of −0.2 dB and high return loss of −19 dB.

2.4. Design of DMTL phase shifter

Based on the previous investigation, it is found that Phase Shifter-II exhibits improved performance compared to others and is therefore chosen for further development. There are two improved designs of DMTL. Firstly, the Phase Shifter-IV employs 11 shunt capacitance switches which have length of 700 μm and width of 90 μm. The switches are equally spaced at 500 μm on the CPW 65 Ω and placed above a transmission line with a total length of 7 mm. Secondly, the Phase Shifter-V employs 16 shunt capacitance switches which have length of 700 μm and width of 90 μm are equally spaced at 300 μm on a CPW 65 Ω above a transmission line with length of 7 mm. The size of these improved designs is smaller than the previous phase shifters where they show an improvement in terms of phase and impedance. A comparison of DMTL phase shifters which are designed with different spacing and number of bridges on high resistivity silicon wafer are shown in Table 2.

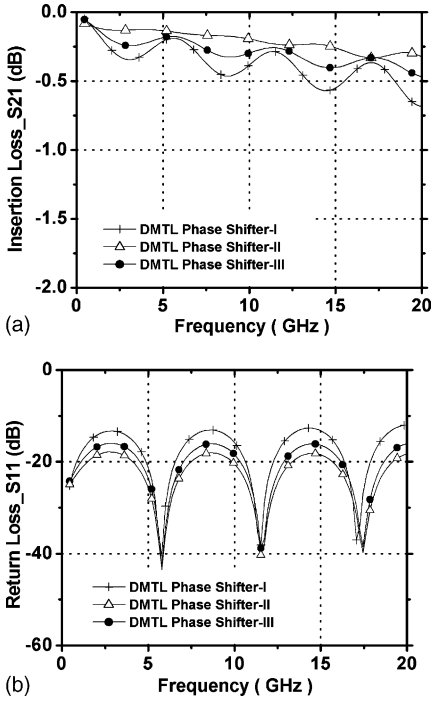

Fig. 6. Characterizations of the three-types of DMTL phase shifters in the up-state (a) insertion loss and (b) return loss.

3. Fabrication processes

The DMTL phase shifters are fabricated on a 675 μm-thick of high resistivity silicon substrate ($\varepsilon_r = 11.9$) using the surface micromachining technology. The configurations of the shunt capacitance switch over CPW transmission line and DMTL are shown in Fig. 1.

The detailed stages of the fabrication process flow for the DMTL phase shifter with the shunt capacitive switch are shown in Fig. 7. First, Fig. 7a shows the deposition of 300 Å/0.5 μm thermal silicon dioxide and PECVD silicon nitride as buffer layer. Next, Fig. 7b shows the deposition of 1.5 μm thick of gold (Au) which is patterned as CPW. Then, in Fig. 7c, there is a deposition of 1500 Å PECVD silicon nitride and is patterned as a dielectric layer between CPW and bridge. After that, a 2 μm thick of photoresist is coated and patterned as a sacrificial layer and this is shown in Fig. 7d. Later, a 1.5 μm thick of aluminum (Al) film is evaporated and patterned to form the bridge and is shown in Fig. 7e. Finally, Fig. 7f shows the dry release of the bridge and capacitive shunt switch is formed. The performance of the switch depends significantly upon some critical parameters, such as the thickness of the metal membrane, the height of the bridge and the residual stress of the metal. Scanning electron microscope (SEM) micrograph of the fabricated DMTL phase shifter and the enlarged view are illustrated in Fig. 8.

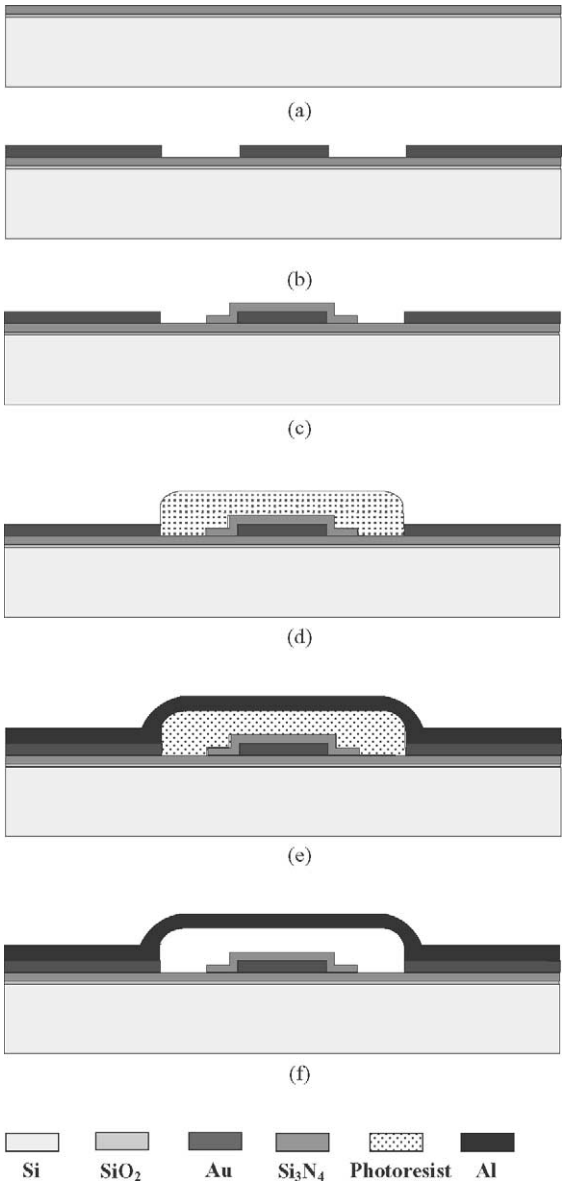

Fig. 7. Details of the fabrication process flow.

4. Experimental results and discussions

The DMTL measurements and characteristics were made using HP8510C network analyzer and calibrated using the short-open-load-through (SOLT) on-wafer standards. The measurement results of the Phase Shifter-II are shown in Fig. 9a and b compared to the simulation results. The measured insertion loss and return loss with various bias voltages are shown in Fig. 10a and b. These results show that a maximum phase shift of 148° at 20 GHz is achieved with 2 dB insertion loss and less than −15 dB return loss. The up-state capacitance of the shunt switch is calculated as 58 fF, with a series resistance of 0.1 Ω and a series inductance of 20 pH (which does not have an effect at X-band), which agrees well with the measured results. The measured shunt switch capacitance is 48 fF due to the residual stress in the bridge. Compar-

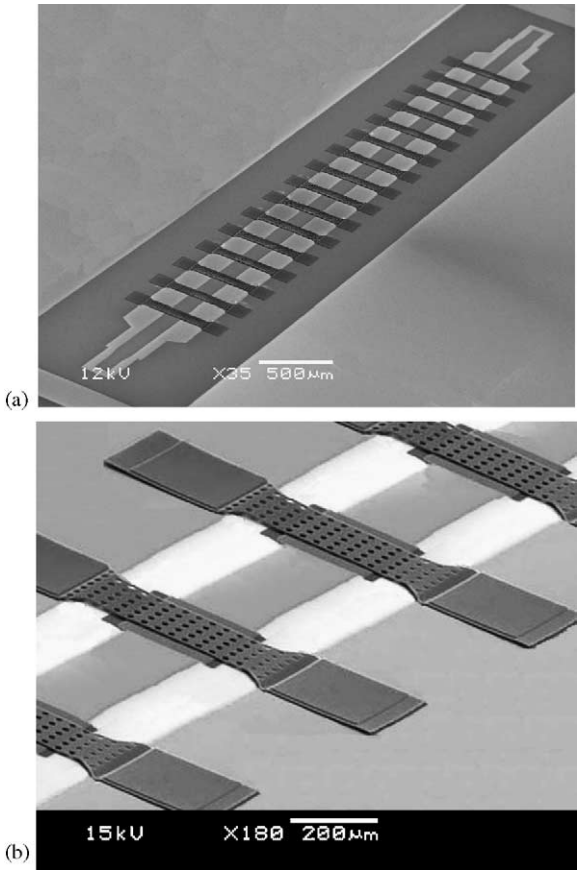

Fig. 8. SEM micrograph of DMTL phase shifter (a) over view and (b) zoom view.

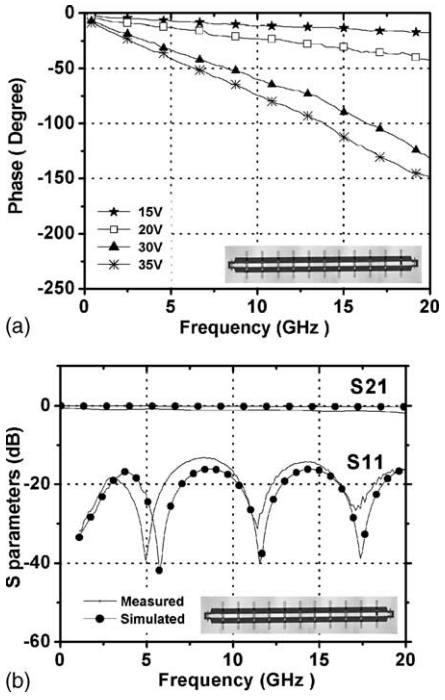

Fig. 9. DMTL Phase Shifter-II (a) measured results of phase shift at different voltages and (b) measured and simulated results of S-parameters.

ison of the three different types design of CPW transmission line is shown in Fig. 6 where Phase Shifter-II achieves the best experimental results with lower insertion loss, higher return loss and larger phase shift as shown in Table 1.

The phase shift obtained is linear with frequency up to 20 GHz. When the bias voltage is increased, the line impedance reduces from 52 Ω at 0 V to 46 Ω at 35 V due to the increase in the capacitive loading of the line as shown in Figs. 2 and 10. The increased loading raises the bridge capacitance from C_{tu} = 58 fF at 0 V to C_{td} = 103 fF at 35 V. In this design, the capacitance ratio, C_r is 1.8. It can be seen that the shunt switch with high capacitance ratio varactor 1.5–2.5 results in a large loading on the CPW transmission line and therefore a large phase shift. The measured DMTL results are excellent with return loss ≤ -15 dB up to Ku band in both the up- and down-state as shown in Figs. 9 and 10, in which the measured result agree well with the simulations results (Fig. 11).

Based on the experimental results of the DMTL Phase Shifter-IV, the insertion loss is below −2 dB along Ku band with the return loss below −15 dB as shown in Fig. 12a and b for different bias voltages. A maximum phase shift of 180° at 20 GHz is shown in Fig. 11. Besides, the phase shift is determined by the impedance change of the DMTL, which also determines the reflection coefficient of the phase shifter. Therefore, DMTL Phase Shifter-V was also tested to improve the impedance changes. The DMTL Phase Shifter-V can achieve a maximum phase shift of 250° at 20 GHz as shown in Fig. 13, which is higher than DMTL Phase Shifter-IV. The comparisons of the improved designs are shown in

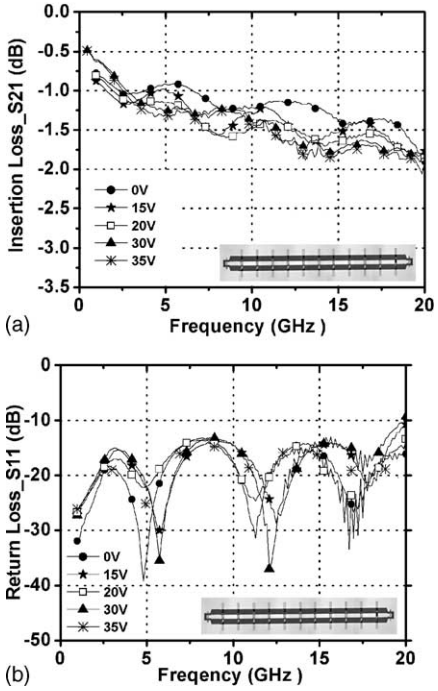

Fig. 10. Measured results of DMTL Phase Shifter-II at different voltages (a) insertion loss and (b) return loss.

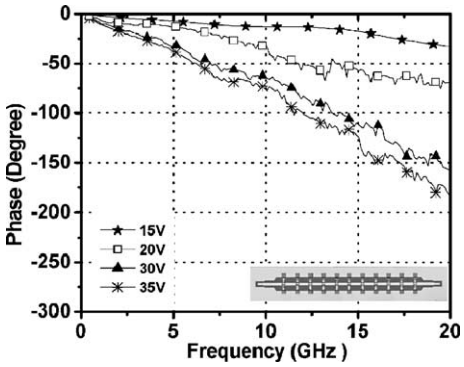

Fig. 11. Measured phase shifts of DMTL Phase Shifter-IV at different voltages.

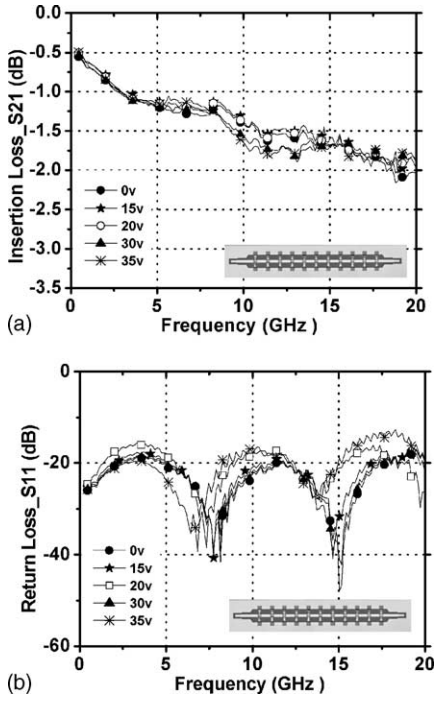

Fig. 12. Measured results of DMTL Phase Shifter-IV at different voltages (a) insertion loss and (b) return loss.

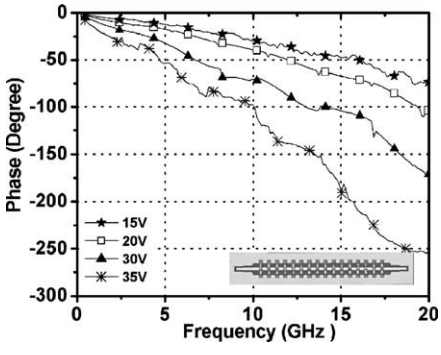

Fig. 13. Measured phase shifts of DMTL Phase Shifter-V at different voltages.

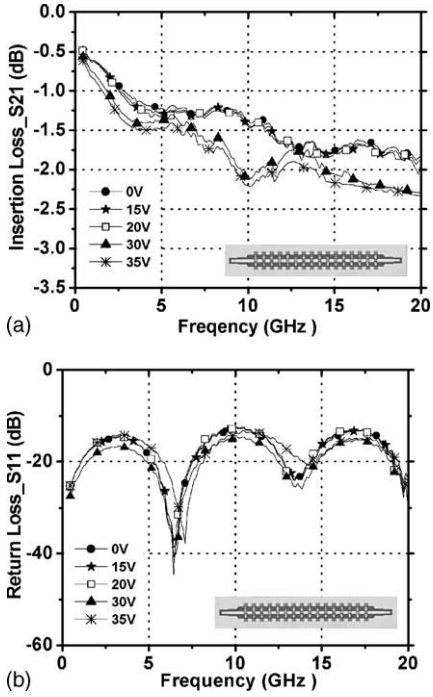

Fig. 14. Measured results of DMTL Phase Shifter-V at different voltages (a) insertion loss and (b) return loss.

Table 2. The measured results of both insertion loss and return loss at different bias voltages are shown in Fig. 14a and b, respectively. From these results, a maximum phase shift of 250° at 20 GHz is achieved with 2.3 dB insertion loss and less than −15 dB return loss.

5. Conclusion

In this paper, the CPW distributed MEMS transmission line phase shifter based on capacitance shunt switch is designed, simulated and fabricated using the surface micromachining processes. The optimal CPW 65 Ω DMTL phase shifters which are measured over very wideband can improve phase shift from 148 to 250°. They remain linear in maintaining return loss ($S_{11} \leq -15$ dB) up to Ku band without discontinuity and integration with other components in the transmission line. The Phase Shifter-II has demonstrated to obtain a maximum phase shift of 148° at 20 GHz with 2 dB loss using 11 shunt capacitance switches. The driving voltage reduces the height of the switches, thereby increases the capacitive loading and decreases the phase velocity. The Phase Shifter-V achieves higher phase shift of 250° at 20 GHz with 2.3 dB loss using 16 shunt capacitance switches. The DMTL can be used as a TTD phase shifter by applying a single analog control bias voltage to the center conductor of the CPW transmission line. As a result, the advantages of the DMTL phase shifters in Ku band are lower insertion loss, higher phase shift and easier integration into RF circuit and systems for different military and commercial applications.

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